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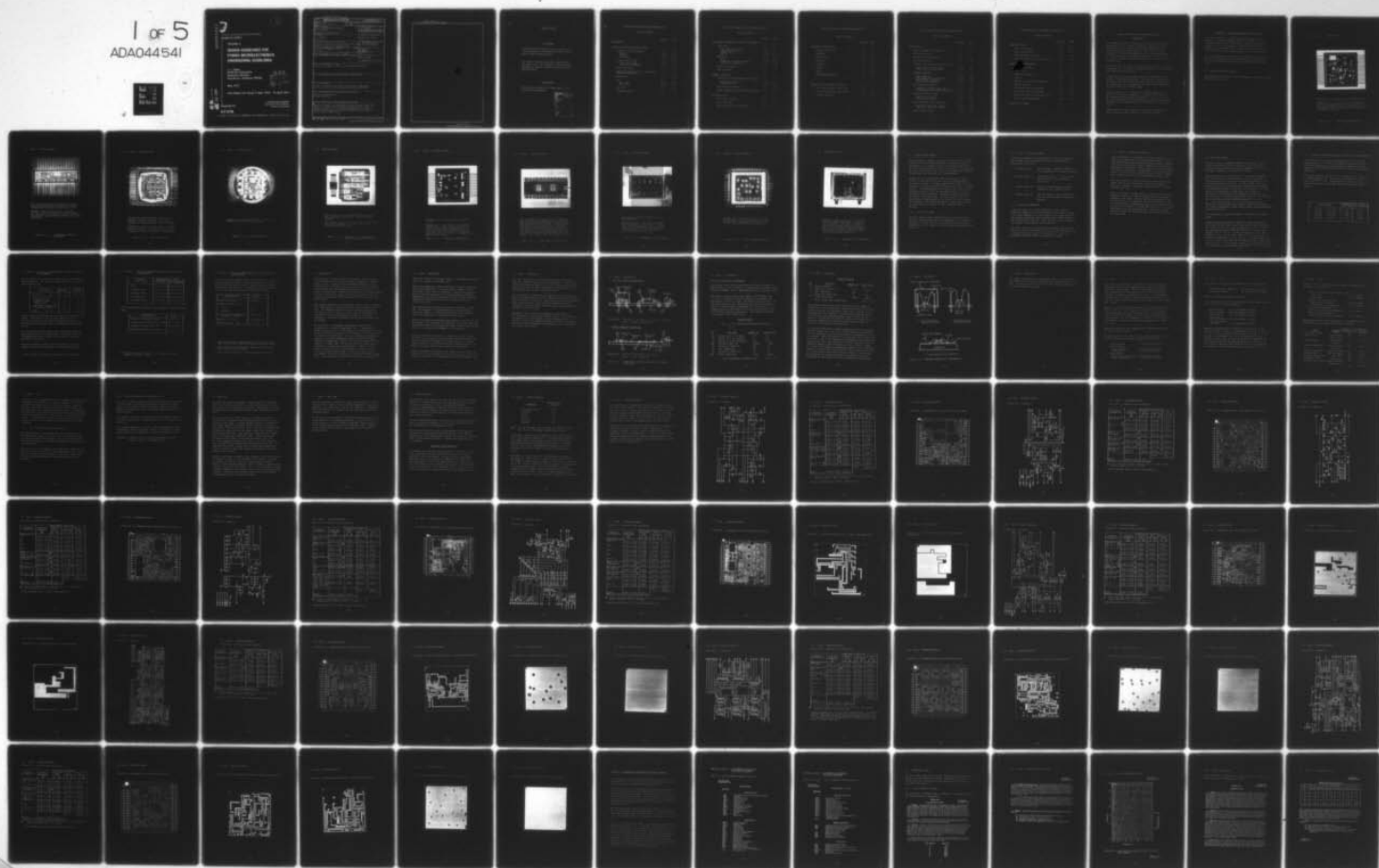
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Research and Development Technical Report
ECOM-76-1358-F

VOLUME II

**DESIGN GUIDELINES FOR
HYBRID MICROELECTRONICS
(ENGINEERING GUIDELINES)**

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May 1977

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DESIGN GUIDELINES FOR HYBRID MICROCIRCUITS

INTRODUCTION

This document delineates guidelines for the design of hybrid microcircuits. Its content is primarily intended to serve as groundrules to be followed by the hybrid layout designer in the design of hybrid microcircuits. However, there is no intension to teach layout design as such. The presumption is made that the reader can interpret electrical schematics and is already competent in printed circuit board or other types of layout design.

The text of this document is divided into categories of design considerations. The Table of Contents indicates those categories and subdivisions within each.

A large portion of this document describes manufacturing technology in a generalized fashion. This general information is included in the belief that the layout designer is better able to evaluate his own design when he is aware of the fundamental processes employed in manufacturing.

Only in a minority of instances can a design simultaneously meet all of the ideal groundrules. Tradeoffs must typically be considered between various groundrules. It is in the area of design tradeoffs that the knowledge of processes serves the designer well in enabling him to set priorities on the groundrules.

Another intent of this document is to provide information to help in the decision of whether or not to use hybrids.

SECTION 1 CIRCUIT EVALUATION AND PARTITIONING

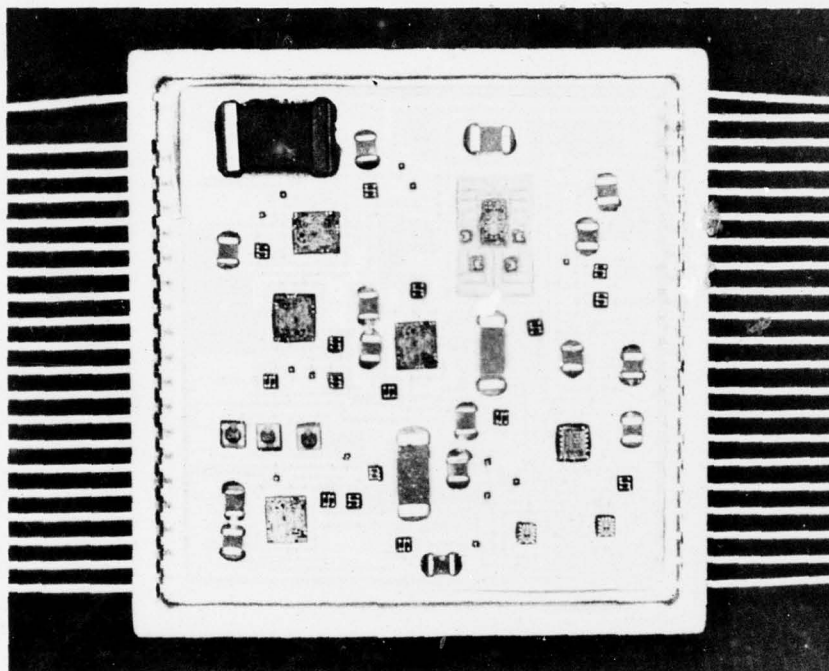
All major categories of electronics have employed hybrid packaging. High speed analog and digital circuits as well as microwave modules can be "hybridized". Besides the obvious reductions in size and weight which hybrid technology can achieve at the component level, there can also be significant size, cost and reliability improvements on the system level.

It is the intention of this section to provide information to aid the packaging engineer in making the decision of whether or not to utilize hybrids; and how to approximate hybrid package sizes.

1.1 EXAMPLES OF HYBRID PACKAGES

The following are examples of hybrid packages for analog, digital, and microwave circuits.

1.1.1 (Cont.) ANALOG CIRCUITS

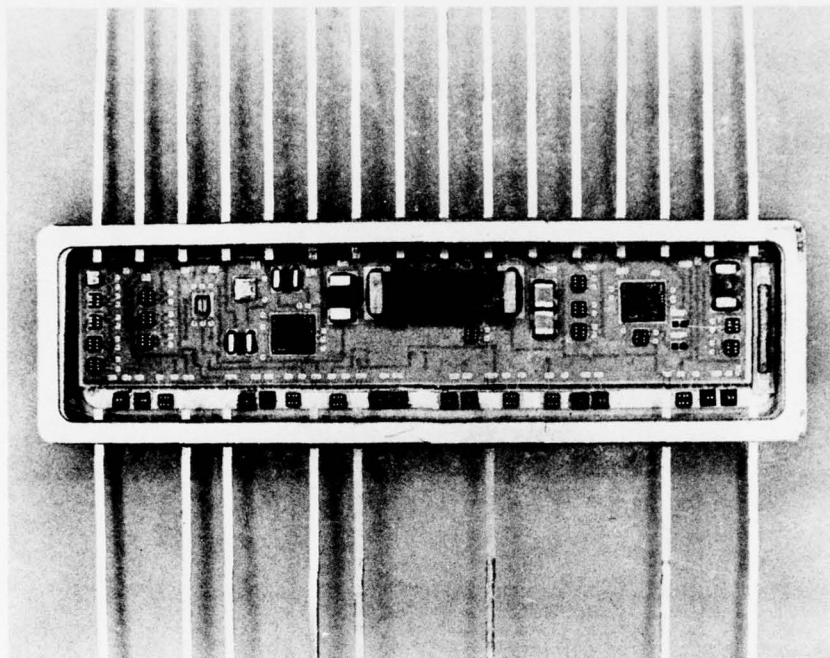


Unit monitors gyro wheel power and rundown time.

Package size 1.1 x 1.1 in. (27.9 x 27.9 mm) gold plated kovar. Multilayer thick film substrate has three conductive layers. Mini-substrate is preassembled and pretested prior to being installed onto mother substrate.

Figure 1.1.1-1 GYRO-WHEEL POWER MONITOR

1.1.1 (Cont.) ANALOG CIRCUITS

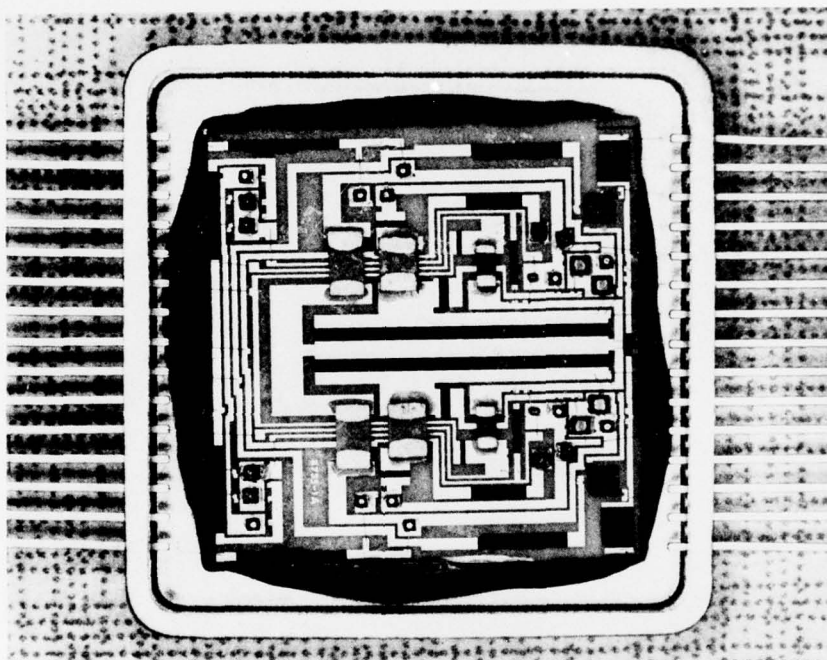


Unit responds to external temperature sensor. Internal transistors act as heaters to control temperature of mounting surface within $\pm .01^{\circ}\text{C}$.

Package is 0.5 x 1.75 in. (12.7 x 19.0 mm) berylia. Thick film multilayer substrate does not completely fill package. Several transistor and resistor chips are mounted directly onto base of package.

Figure 1.1.1.-2 TEMPERATURE CONTROLLER
AND HEATER

1.1.1 (Cont.) ANALOG CIRCUITS

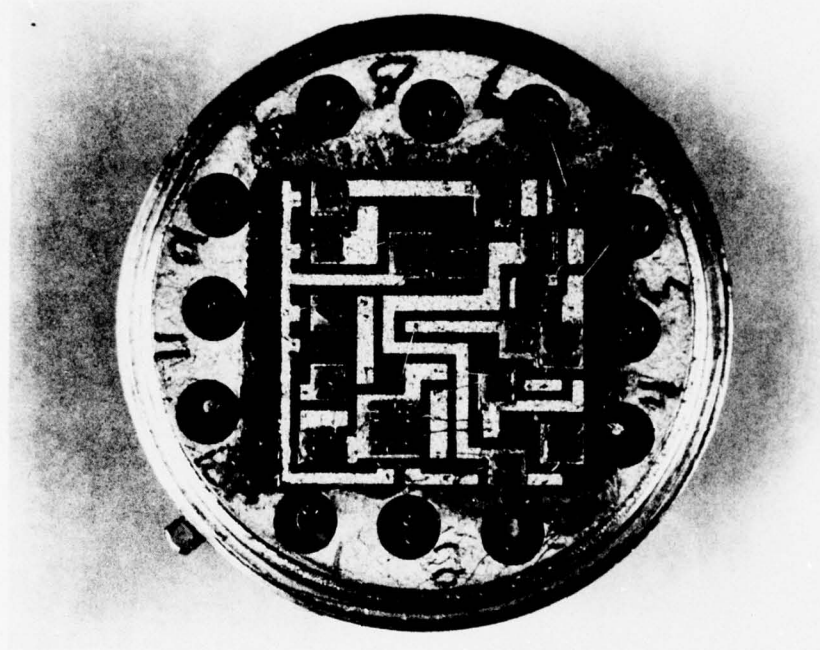


Two identical inhibit driver circuits in one package. Resistor tolerances $\pm 1\%$. Two resistors matched within 0.1%. Four resistors dynamically trimmed to adjust offset voltage.

Package size is 1.0 x 1.0 in. (25.4 x 25.4 mm) gold plated kovar. Thin film substrate with resistors integral to substrate. Later version converted to single layer thick film substrate.

Figure 1.1.1-3 DUAL INHIBIT DRIVER

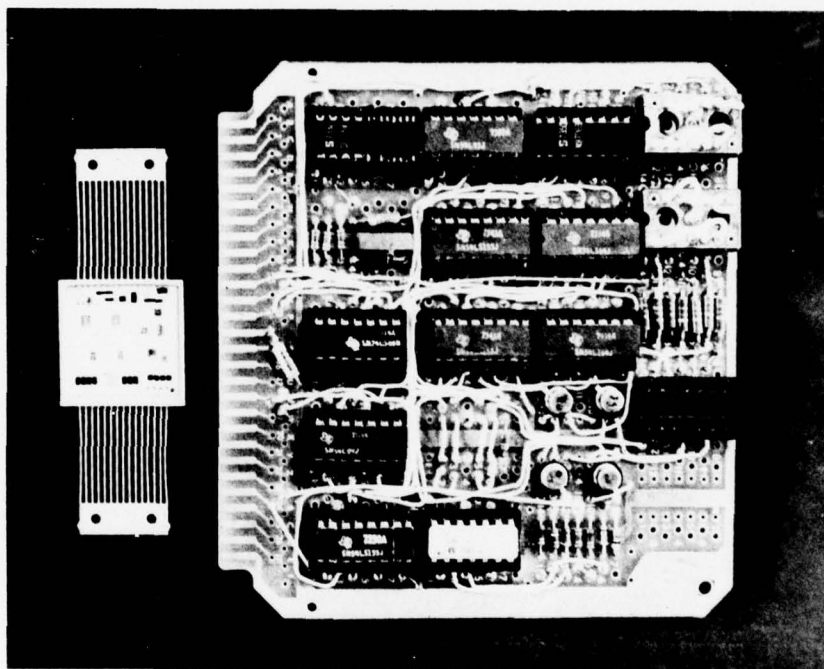
1.1.1 (Cont.) ANALOG CIRCUITS



Package is twelve pin TO-8 header. Metal cover hermetically seals onto rim of header.

FIGURE 1.1.1-4 VOLTAGE REGULATOR

1.1.2 DIGITAL CIRCUITS

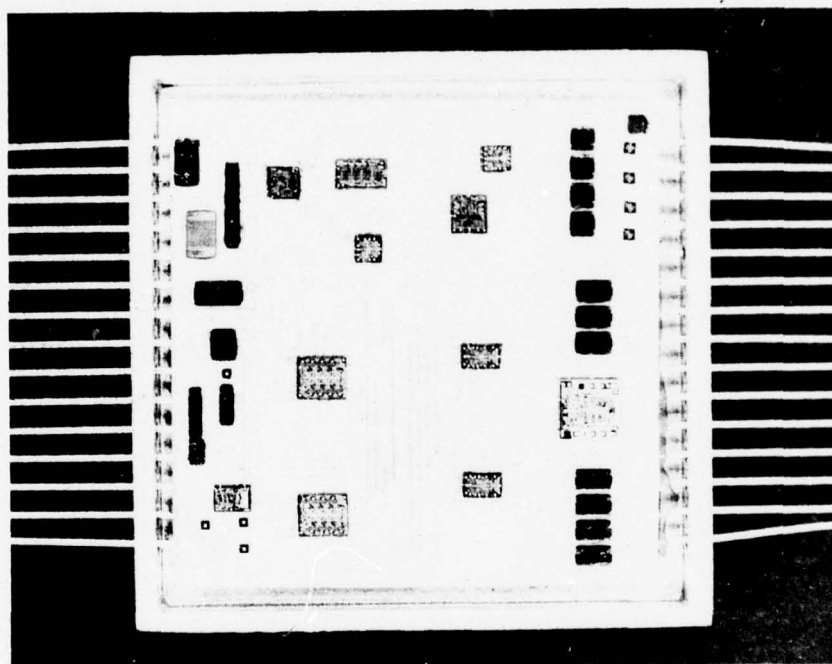


Unit converts serial digital data into parallel BCD and displays onto LED's. Control functions included.

P.C. Board size is 6.9 x 7.3 in. (175.3 x 185.4 mm).
Microcircuit package is 1.0 x 1.0 in. (25.4 x 25.4 mm) gold plated kovar.

FIGURE 1.1.2-1 SENSOR LOG (P.C. BREADBOARD AND FINAL MICROCIRCUIT PACKAGE)

1.1.2 (Cont.) DIGITAL CIRCUITS

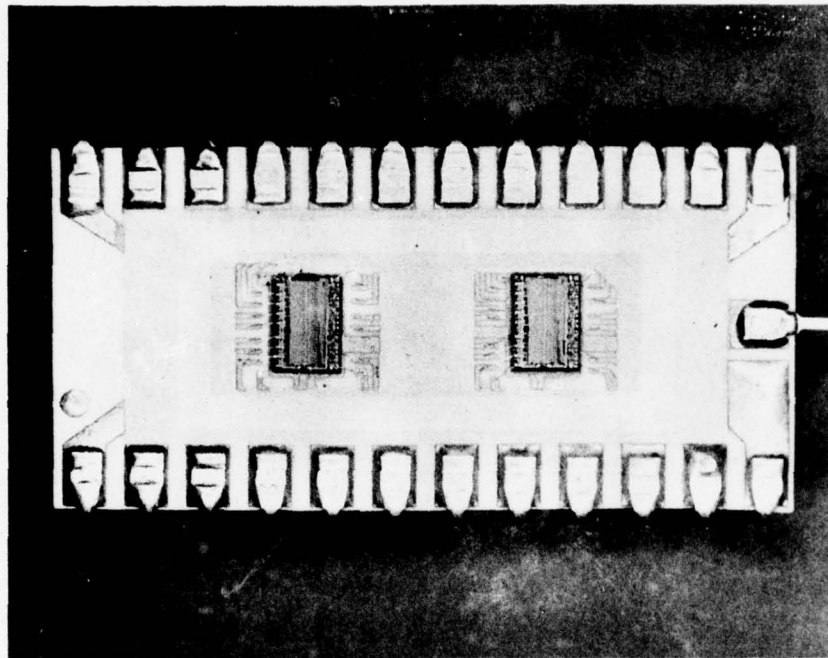


Enlarged view of microcircuit from Figure 1.1.2-1.

Package is 1 x 1 in. (25.4 x 25.4 mm) gold plated kovar. Thick film substrate with three layers of interconnecting tracks in central portion only. Single layer in the areas where the resistors are screened on. Resistors tolerances are $\pm 5\%$. No multilayer under the I.C. chips.

Figure 1.1.2-2 SENSOR LOG (MICROCIRCUIT)

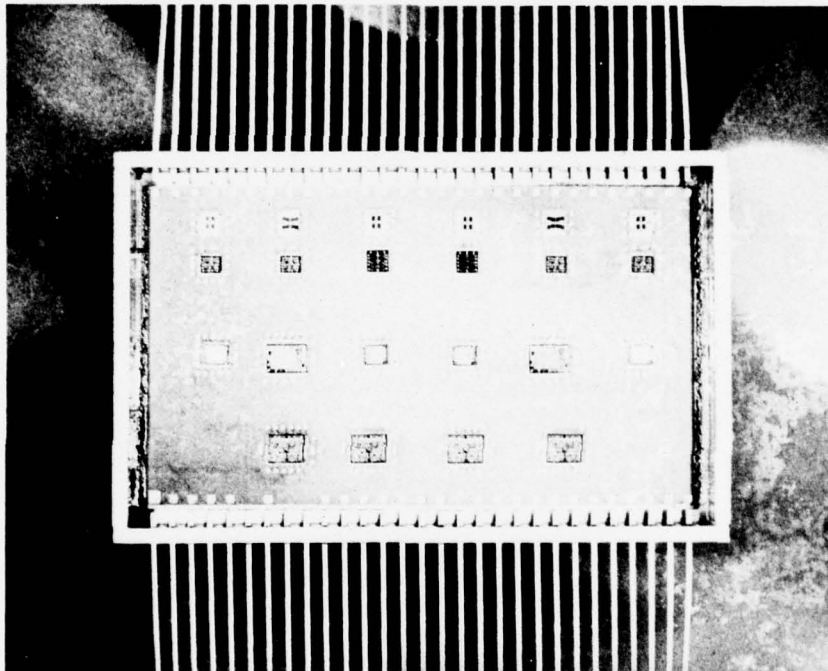
1.1.2 (Cont.) DIGITAL CIRCUITS



Size is standard 24 lead dual-in-line package. Unit consists of two PROM chips on a thick film multilayer substrate with leads solder-attached over the edges of the substrate. Package shown with plastic cover removed. Later version of same unit has PROM's individually prepackaged in hermetically sealed carrier packages in order to facilitate testing and programming prior to the carriers being mounted onto the mother substrate. No cover required in the later version.

Figure 1.1.2-3 ALPHA NUMERIC DISPLAY DRIVER

1.1.2 (Cont.) DIGITAL CIRCUITS

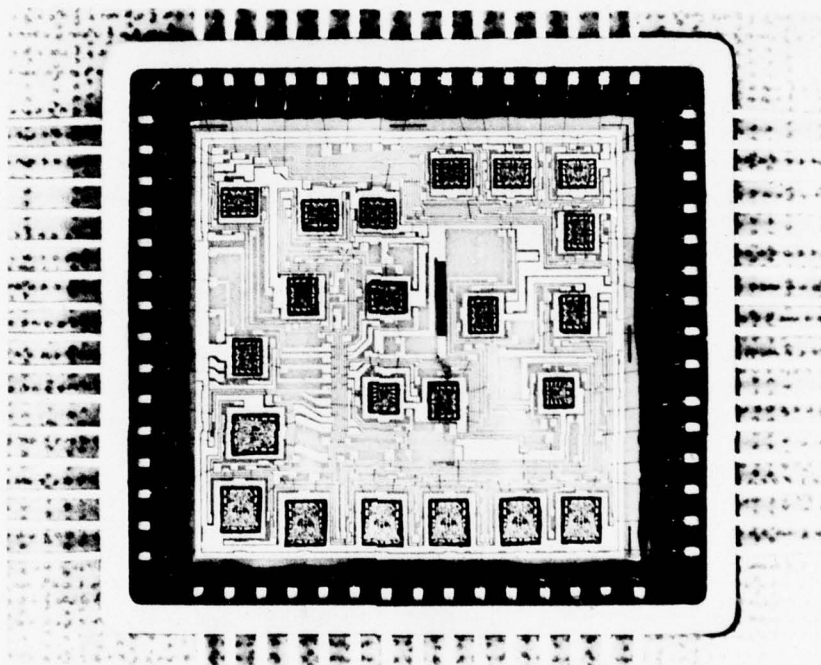


Unit outputs a prescribed pulse at a pre-programmed time.

Package is 1.0 x 1.5 in. (25.4 x 38.1 mm) gold plated kovar. Substrate is a multi-layer thick film with two layers for inter-connecting tracks and one each ground and voltage planes. For easier wiring, only wire bond pads are on top layer.

Figure 1.1.2-4 PROGRAMMABLE PULSE GENERATOR

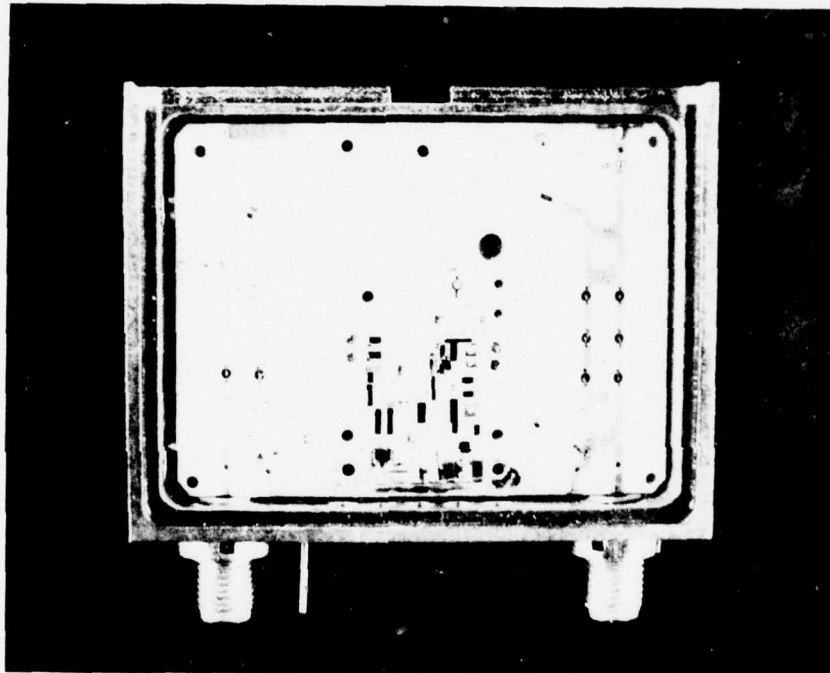
1.1.2 (Cont.) DIGITAL CIRCUITS



Package size 1.0 x 1.0 in. (25.4 x 25.4 mm)
gold plated kovar with fifteen leads on each
of four sides. Substrate is thin film with
2.5 mil interconnecting tracks and spaces.

Figure 1.1.2-5 I.M.U. COMMUNICATIONS LOGIC

1.1.3 MICROWAVE CIRCUIT



Package is 1.8 x 2.2 in. (45.7 x 55.9 mm) plated aluminum with connectors sealed into side walls. Thin film substrate has couplers built into conductive pattern. Pin diodes are mounted into plated-through holes in the substrate. Mini-substrate is preassembled and pretested prior to being installed onto mother substrate.

Figure 1.1.3-1 AUTOMATIC LEVEL CONTROLLER

1.2 CIRCUIT PARTITIONING

In partitioning a complex circuit or system, one key consideration is that each portion should be a functional entity. If each "block" of a complex system is an integral function, it not only can be replaced as a unit but can also be tested prior to being installed into the system. This philosophy should be incorporated into the design of a hybrid module.

Another obvious consideration when partitioning a complex circuit, is how much can be put into one assembled package. Unfortunately there is no known quantitative ground rule that accounts for all the variables influencing the size of a hybrid circuit. The quantitative rules given in the section called "Packaging Density" allow for the quantity and size of the components but do not address themselves to the requirements for complex interconnections. Personal judgement must be applied when estimating the area or number of layers needed to accommodate interconnecting tracks. Examples are provided for comparisons of circuits to their completed hybrid designs.

1.2.1 Level of Assembly

The most common assembly level build-up, using hybrid micro-circuits, proceeds from the micro-components within the hybrid package; to several hybrids, along with discrete components, mounted onto a P.C. board; to several boards being mounted into a chassis.

1.2.1 (Cont.) Level of Assembly

In order to provide for quick reference in the following text, the assembly levels mentioned above are assigned arbitrary designations as follows:

Assembly level I	The individual component, whether a micro-component or a discrete component.
Assembly level II	The hybrid module. In this context, when hybrids are not used there is no level II.
Assembly level III	The P.C. board containing discrete components and/or hybrid modules.
Assembly level IV	The next assembly level higher than the P.C. board, usually a mechanical housing.

1.2.2 Functional Complexity

A word of caution is in order pertaining to the degree of functional complexity to be incorporated into a single hybrid. It is often tempting to use the largest size package available and thereby incorporate into one package what might otherwise have required more than one. There can be a point of diminishing returns if this idea is carried too far.

The yields that can be realized in the substrate fabrication processes are often affected by the size of the substrate. Many of the processes work best on flat surfaces. As the size increases, the total effect of curvature is greater.

1.2.2 (Cont.) Functional Complexity

Very significant, in the trade-offs to be considered, is the ability to functionally test the completed hybrid. It has been demonstrated that incorporating overly complex functions into one unit has caused greater complexity in the testing equipment and procedures. Fault isolation is more difficult when greater complexity is encountered. As a generalization analog circuits (especially high frequency circuits) require more careful scrutiny in this regard than do digital ones.

Recycling a hybrid to remove and replace one defective component subjects the entire unit to the risk of damage. Excessive crowding of components inside the hybrid, greatly increases the risk.

Since each design is unique there is no precise quantitative ground rule that can establish optimum trade-offs between complexity and yields. The one rule to be respected is that the question of over complexity should not be ignored. Electrical performance, manufacturing processes, testing and reworking can all be adversely affected when too many or too complex requirements are imposed on one unit. Expertise in those categories should be applied when the partitioning decisions are being made.

1.3 WEIGHT AND VOLUME

The use of Level II packaging (hybrid microcircuits) reduces weight and volume not only by comparison to the identical circuits being packaged with discrete components, but also at the higher assembly levels (Levels III and IV).

The higher densities achieved at Level II reduce the number of Level III PC boards, and the number of Level IV connectors, interconnecting wires, and associated mounting hardware. The following case makes the point. A radar antenna controller system using all discrete components required eleven PC boards with components mounted on both sides of each board. The same system utilizing hybrids, along with a few discretes, required only seven boards with components on only one side of each board. The first eleven boards weighed 11 lbs. (4.9 kg). The seven boards utilizing hybrids weighed 4.6 lbs. (2.1 kg). After "hybridizing", the system housing was able to accommodate two additional subassemblies (which would otherwise have occupied additional volume and would have required additional mounting provisions).

The following is a specific example of the weight of a hybrid module.

A hybrid module consisting of several IC chips, capacitors, transistor and diode chips, and a multilayer ceramic substrate all within a 1.0 x 1.0 x .150 in. high (25.4 x 25.4 x 3.81 mm) kovar package having 30 leads and sealed with a kovar cover weighed .264 oz. (7.5 g). The kovar package and cover alone weighed .215 oz. (6.1 g), which means that the electronics and substrate weighed only .049 oz. (1.4 g). A ceramic package 1.0 x 1.0 in. (25.4 x 25.4 mm) with 30 leads and a kovar cover weighs .176 oz (5.0 g). If the ceramic package were substituted for the kovar package, the total module weight would be 225 oz. (6.4 g).

1.4 ELECTRICAL CHARACTERISTICS OF THIN AND THICK FILM MATERIALS

The electrical characteristics presented in this section are generalizations. It should be recognized that materials from different manufacturers will have unique properties and that changes in substrate fabrication processes can vary the material properties.

Thin film conductor material is most commonly gold. The purity is approximately 99.9%. The electrical resistivity is typically $2.44 \times 10^{-6} \Omega \text{ cm}$. Translating this figure into the 5-mil wide configuration of the common thin film conductor tracks gives,

GOLD THICKNESS	RESISTANCE/UNIT LENGTH	
	ONE INCH	ONE CENTIMETER
50 $\mu\text{in.}$ (1.27 μm)	3.86 Ω	1.52 Ω
100 $\mu\text{in.}$ (2.54 μm)	1.93 Ω	0.76 Ω
150 $\mu\text{in.}$ (3.81 μm)	1.28 Ω	0.51 Ω
200 $\mu\text{in.}$ (5.08 μm)	0.96 Ω	0.38 Ω

1.4 (Cont.) ELECTRICAL CHARACTERISTICS OF THIN AND THICK FILM MATERIALS

The two common thin film resistor materials are nichrome and tantalum nitride. The common characteristics for resistors of these materials are

CHARACTERISTIC	NICHROME	TANTALUM NITRIDE
Resistivity Ω/\square	25 - 250	100 - 600
Processing Accuracy (%)	± 10	± 10
Trimming Accuracy:		
Automatic Laser (%)	$\pm .01$	$\pm .01$
Manual Laser (%)	± 1	± 1
Temperature Coefficient of Resistance (PPM/°C)	≤ 50	≤ 100
Stability: (% ΔR)	.01 ^{L1}	.005 ^{L1}

Several conductive materials are available for thick film substrates. Gold paste is the one most commonly used for military applications, but other frequently used pastes are palladium gold, palladium silver, platinum gold and platinum silver.

The values shown presume that the processing steps meet the paste manufacturer's recommendations. Deviations from those recommendations produce various effects, some of which are mentioned in Section 6.2

Conductive materials, when used in the common 10-mil wide conductor tracks, have properties in the following ranges.

^{L1} Lower values can be achieved with glaze over resistors.

1.4 (Cont.) ELECTRICAL CHARACTERISTICS OF THIN AND THICK FILM MATERIALS

MATERIAL (10 mils wide)	RESISTANCE/UNIT LENGTH	
	ONE INCH	ONE CENTIMETER
Gold	0.2 to 0.5 Ω	0.08 to 0.2 Ω
Platinum Gold	2.5 to 10.0 Ω	1.0 to 4.0 Ω
Platinum Silver	0.15 to 0.25 Ω	0.06 to 0.1 Ω
Palladium Gold	2.0 to 10.0 Ω	0.8 to 4.0 Ω
Palladium Silver	0.5 to 6.0 Ω	0.2 to 2.4 Ω

Thick film dielectric materials have properties in the following ranges.

CHARACTERISTIC	VALUE
Dielectric Constant (@ 1kHz) ^{L1}	8 to 20
Insulation Resistance (Ω @ 100 VDC)	10^9 to 10^{12}
Breakdown Voltage (Volts DC)	500 to 1,000
Dissipation Factor (% @ 1 kHz)	<1 to >3

^{L1} Dielectric materials intended for capacitors can have constants as high as 2,000.

1.4 (Cont.) ELECTRICAL CHARACTERISTICS OF THIN AND THICK FILM MATERIALS

Thick film resistor materials have a wide variety of resistivities and other properties. High resistivity pastes usually exhibit different characteristics from the lower value pastes. The following information is a compilation of the characteristics to be expected from thick film resistor pastes.

CHARACTERISTIC	VALUE
Processing Accuracy (%)	20 to 30
Trimming Accuracy: (%)	
Laser	± 0.1
Abrasive	± 5
Temperature Coefficient of ^{L1} Resistance (PPM/°C)	50 to 700
Stability: (% Δ R) ^{L2}	as low as 0.1
Quan-Tech Noise: (dB) ^{L3}	-30 to 0

^{L1} Some materials have a negative TCR in the low temperature range and a positive TCR in the higher temperature range.

^{L2} Varies significantly with paste composition; also varies with resistor size and shape.

^{L3} Varies with resistor size, shape and sheet resistivity.

1.5 RELIABILITY

An evaluation of hybrid reliability should be directed toward all the assembly levels, from individual components to the complete system. Considered as an individual component, a semiconductor device intended for use in a hybrid may be rated less reliable than that same component prepackaged for use on a PC board; a hybrid module compared to an equivalent PC board assembly, may have a reliability rating less than the PC board; yet the system rating might be better with the same hybrids rather than without them.

The standard procedures for calculating failure rates are spelled out in MIL-HDBK-217; revision B of Sept. 1974, updated in Sept. 1976. The handbook dictates not only calculating procedures and generic failure rates for various types of components and connections, but also allowances to be made if individual component is pretested ("stressed") before being installed into an assembly.

In pretesting, a prepackaged semiconductor typically has an advantage over a "naked" (unpackaged) one. A semiconductor installed and wired in its own package can be subjected to environmental stresses and electrical tests that are, at best, difficult to achieve with naked chips. In an air atmosphere, prolonged exposure to elevated temperatures sometimes has deleterious effects on a naked chip. Probes must be used to make electrical contact to a naked chip, yet the electrical resistance at the interface of a probe and a terminal pad is often too high to permit sensitive electrical measurements. Probing can also scratch the chip metallization. For these and other reasons, environmental and analog pretesting is seldom performed on naked chips. They typically are only DC tested by their manufacturer.

1.5 (Cont.) RELIABILITY

Chips that receive this minimal amount of preassembly testing are rated less reliable by MIL-HDBK-217B.

Because the components within a hybrid are in much closer proximity, the thermal density is higher than it would be if the equivalent circuit were on a PC board. Because the density is greater, hybrid components will experience higher operating temperatures than on an equivalent PC board. Higher operating temperatures considerably lessen the reliability of any electrical device.

Some important ways that hybrids improve reliability is that they can withstand very high mechanical stresses and they reduce the number of connections between different materials. (Each such connection is a potential failure point.)

Hybrids can typically withstand high mechanical stresses, because the weight of the materials and components is so small that even when their weights are multiplied by large g loads, the resultant forces do not exceed the strengths of the materials.

A quarter-watt film resistor on a substrate has only a small fraction of the weight of an equivalent discrete resistor; and the film resistor is bonded to the substrate over its entire surface, while for the discrete resistor, attached only by its leads, any forces applied create stresses in the leads.

Naked semiconductors attached to the substrate do not have the weight of a discrete package; and a discrete package would also cause all the stress to be concentrated in the attachment leads.

1.5 (Cont.) RELIABILITY

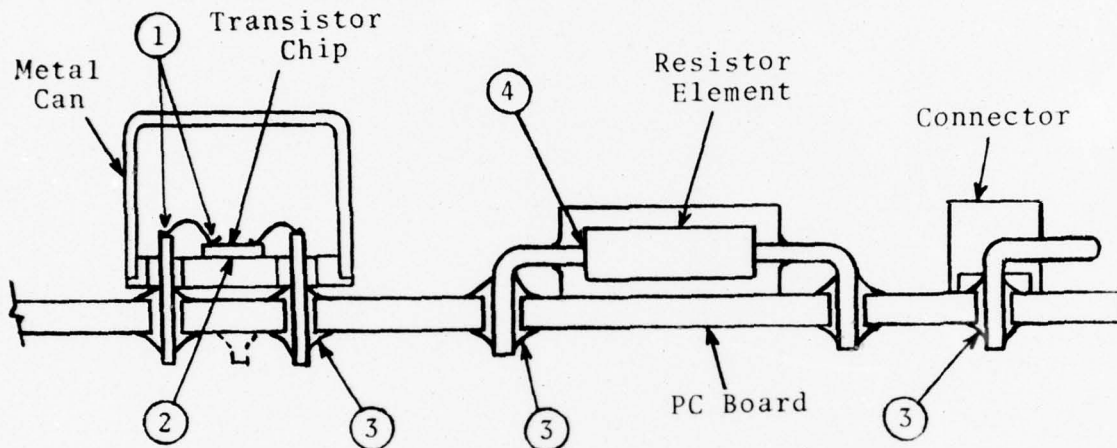
One other significant way that hybrids improve reliability is that they eliminate many electrical connections. Consider the comparisons shown in Figure 1.5-1 of a PC board converted into a hybrid. Not only are there fewer bonds in the hybrid, but the type ⑤ bond on the hybrid is highly reliable.

This reduction of connections also happens at the system level. Because the hybrid packaging is so much denser than the discrete, fewer PC boards are required. Fewer boards means fewer connectors. Fewer connectors means fewer interfaces between board and connector, as well as fewer interconnections between connectors and the rest of the system.

Included are the results of a mathematical evaluation of the reliability of an airborne digital system. This evaluation was done prior to the beginning of the packaging design. It presents a one-to-one comparison between the potential packaging only with discrete components and packaging with a combination of discretely and hybrids.

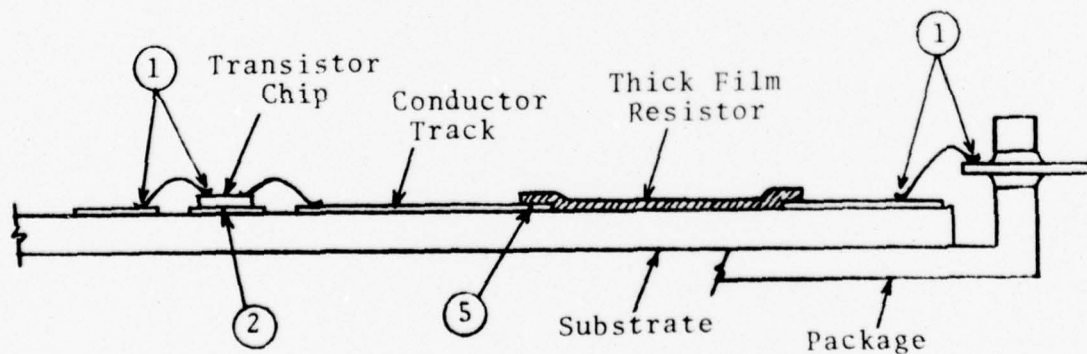
1.5 (Cont.) RELIABILITY

a. Discrete Component Connections



Connections: Four type 1, one type 2, six type 3, two type 4.
Total = thirteen connections

b. Hybrid Component Connections



Connections: Six type 1, one type 2, two type 5.
Total = nine connections

Figure 1.5-1 COMPARISONS OF HYBRID AND DISCRETE COMPONENT CONNECTIONS

1.5 (Cont.) RELIABILITY

Results of Reliability Evaluation

The discrete case failure rate was 88×10^6 hours, whereas the hybrid case was 101×10^6 hours. Considering the accuracy of the predictive method, the two implementations are essentially equal.

The analysis was performed in accordance with MIL-HDBK-217B, Section 3.0 assuming an airborne inhabited environment, and part quality factors as shown. The hybrid circuit failure rate was determined from data supplied by the Hybrid Engineering Supervisor and the model of MIL-HDBK-217B, Section 2.1.7. The thermal analysis showed that the IC die in the hybrid will be 12.4°C hotter than the discrete die. This thermal difference is reflected in the failure rates.

DISCRETE PARTS

IC's: $\pi_Q = 2.5$, MIL-STD-883 Method 5004 Class B

$\pi_L = 1$

<u>QTY</u>	<u>PART TYPE</u>	<u>GENERIC FR</u>	<u>PART TYPE FR</u>
100	Bipolar IC's (1-20 Gates)	.227	22.7
50	Bipolar IC's (21-50 Gates)	.4	20
50	Bipolar IC's (51-100 Gates)	.575	28.75
100	Resistors (RCR---S)	.000048	.0048
40	Capacitors (39003--P)	.033	1.32
10	PCB - Multilayer	.90	9.0
10	Connectors (Mated Pair)	.51	5.1
4280	Solder Connections	.00044	<u>1.8832</u>
TOTAL FAILURE RATE (DISCRETE CASE)			88.8×10^{-6}

1.5 (Cont.) RELIABILITY

HYBRID CIRCUITRY

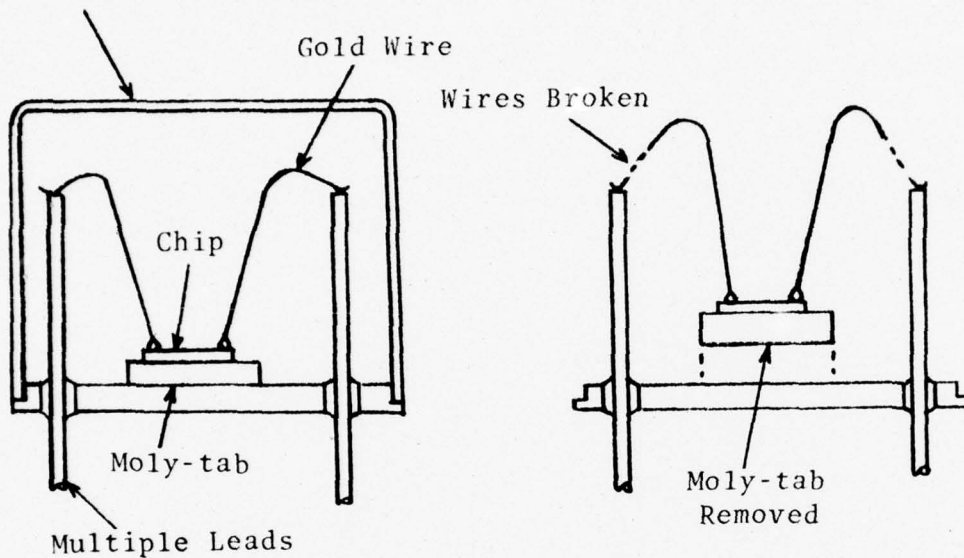
<u>QTY</u>	<u>PART TYPE</u>	<u>GENERIC FR</u>	<u>PART TYPE FR</u>
12	Hybrid Circuits	8	96
12	Capacitors (39003---P)	.033	.792
3	PCB - Multilayer	.90	2.7
3	Connectors (Mated Pair)	.51	1.53
924	Solder Connections	.00044	<u>.4176</u>
TOTAL FAILURE RATE (HYBRID CASE)			101.4×10^{-6}

The evaluation did not include calculations of the number of connections at the system level, because the design of the intra-system wiring was not finalized at that time. However, it was estimated that the reduction of intrasystem connections would still make the two packaging methods close to equal in reliability. The decision was made to use hybrids in order to gain the other advantages of hybrids with the assurance that no sacrifice in reliability was being made.

In the above evaluation the naked semiconductors being assembled into the hybrids were rated less reliable than their counterpart discrete components because no preassembly environmental stressing was assumed. One costly method of prestressing that has been done in the past consists of temporarily prepackaging (and wiring) the semiconductor chip, then stressing it before removing it from its temporary package; then reinstalling it into a hybrid. Figure 1.5-2 shows this temporary prepackaging method. Chips permanently mounted in chip carriers and chips with either integral beam leads or with beam leads added (tape carrier techniques) can provide the capability of pretesting without using probes on the chip metallization, and without the need for temporary prepackaging.

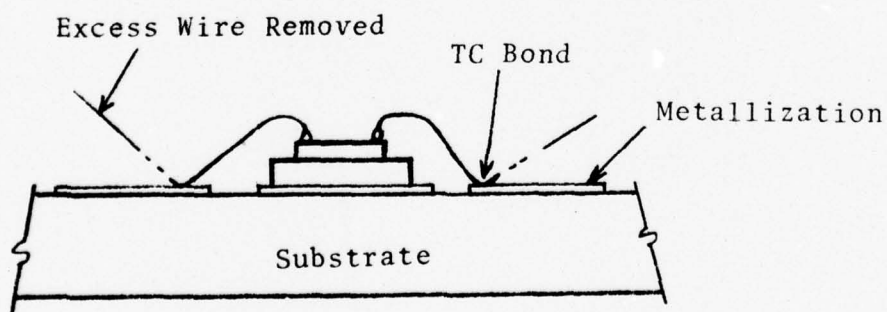
1.5 (Cont.) RELIABILITY

Cover (Temporarily Installed)



a) Chip Installed in Temporary Package

b) Chip Removed from Temporary Package



c) Chip Reinstalled on Substrate

Figure 1.5-2 TEMPORARY PACKAGING OF SEMICONDUCTOR

1.5 (Cont.) RELIABILITY

In comparing thin and thick film hybrids, both TC and ultrasonic wire bonds on thin film are considered more reliable than on thick film. The glass mixed with the thick film gold makes bond integrity more difficult to achieve.

1.6 COST

The following information is intended to give a rough order of magnitude estimate of the manpower hours required for hybrid fabrication and assembly. Of course each hybrid manufacturer has a proprietary pricing method based on processing yields, equipment availability, overhead costs, etc. The information included here is intended to make distinctions between processes that may require several man-hours versus others that may require only seconds.

Material costs are not discussed because of the constant fluctuations in prices. Time estimates for electrical testing are also excluded because of the many variables. (The equipment used for electrical testing can make a great difference in the time required; also if a component is faulty, or a connection is intermittent, a great deal of time may be expended to isolate the fault.)

Man-hour requirements for commonly used assembly processes can be generalized as follows:

Presuming that only one type of die is being installed, the die-attach operations can usually be performed as follows:

Eutectic-attach	75 to 125 die per hour
Solder-attach:	
Using preforms:	35 to 65 die per hour
Using paste:	50 to 80 die per hour
Epoxy-attach:	
Using dispensing machine	50 to 80 die per hour
Manual application	35 to 65 die per hour

1.6 (Cont.) COST

Wire bonding can usually be performed at the following rates:

Thermocompression Bonding	150 to 250 wires per hour
Ultrasonic Bonding	400 to 600 wires per hour

Reminder: Each wire requires two bonds.

Cover sealing can usually be performed at the following rates for 1.00 x 1.00 in. (2.54 mm) packages:

Weld Sealing:	50 to 70 packages per hour
Solder Sealing:	20 to 40 packages per hour
Epoxy Sealing:	20 to 40 packages per hour
Gross Leak Testing (bubbles):	25 to 40 packages per hour
Fine-Leak Testing (helium):	6 to 12 packages per hour

Manually manipulated laser trimming of ten resistors on one substrate should require 15 to 30 minutes to trim to an accuracy of $\pm 5\%$. (Closer tolerances require additional time.) If an automatic, programmable laser is used, ten resistors will probably require eight (8) hours to program the equipment and check the program; the trimming operation will require 20 to 40 seconds for handling each substrate and 5 to 10 seconds for the machine to trim the ten resistors to an accuracy of $\pm 1\%$.

1.6 (Cont.) COST

Estimates of the labor required for commonly performed rework operations are as follows:

Removal of solder or epoxy-sealed cover:

Flat cover	1 to 2 minutes
Other shapes	5 to 15 minutes

Removal of weld-sealed cover:

Machine shop grinding:	25 to 40 minutes
Using specialized equipment:	5 to 10 minutes

Removal and replacement of a

eutectically attached semiconductor:	5 to 20 minutes
--------------------------------------	-----------------

Removal and replacement of a

solder or epoxy attached component:	5 to 20 minutes
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Approximations of man-hour requirements to environmentally and mechanically test one hundred parts are as follows:

<u>Test</u>	<u>Equipment</u>	<u>Quantity Tested Simultaneously</u>	<u>Man-Hours (100 parts)</u>
High Temp. Storage	Oven	100	4 to 8
Temp Cycling	Temp. Chamber (Hot & Cold)	100	4 to 8
Thermal Shock	Liquid Bath Facility	20	6 to 10
Burn-In (operating)	Oven with rack for parts	100	1 to 2
Moisture Resistance	Humidity Chamber	100	4 to 8
Salt Atmosphere	Salt Fog Chamber	100	4 to 8
Constant Acceleration	Centrifuge	20	1 to 2
Mechanical Shock	Shock Tower	24	12 to 16
Variable Freq. Vibration	Electrodynamic Shaker System	24	16 to 24
	Total		<u>52 to 86</u>

1.6 (Cont.) COST

For many of the environmental tests, the paperwork (logging data, checking serial numbers, etc.) and the handling of the parts constitutes a large portion of the time required. Specific man-hour requirements for these tests are also dependent upon the particular test conditions being specified. It should also be noted that if electrical tests are to be performed following certain environmental tests, this would be a significant cost factor. Considering the potential total man-hours, it is not unusual for the cost of testing to exceed the costs for manufacturing.

1.6.1 Thin Film Substrate Fabrication Costs

One common method of fabricating thin film substrates is to produce multiple images on a 2.00 x 2.00 in. (50.8 mm) ceramic. The number of individual substrates that can be obtained from each oversized ceramic is obviously determined by the size of the individual image.

Fifty 2.00 x 2.00 in. ceramics, containing both conductors and resistors can be fabricated in 6 to 10 man-hours. This estimate does not include resistor trimming. Fifty such ceramics containing only conductor patterns can be fabricated in 4 to 7 man-hours.

1.6.2 Thick Film Substrate Fabrication Costs

The cycle of printing, drying, and firing processes is performed for each thick film pattern, regardless of the material being applied or the number of layers involved. However, the time required for the cycle varies significantly between single and multiple layers

Five hundred single layer substrates, using automatic ejection from the screen printer, should require from 2 to 4 man-hours for each cycle.

Five hundred multilayer substrates, with four ~~conductive~~ layers and manually removing each part from the screen printer should require from 10 to 16 man-hours to process through each cycle.

Reminder: A double cycle is typically performed for each dielectric and via-fill application.

1.7 LEAD TIME

The lead time required to produce a small quantity of prototype hybrids can only be estimated as a broad generalization, because many factors can influence this lead time. Nevertheless, a hybrid can generally be designed and prototype units produced within six weeks.

The time required for layout design is influenced not only by the quantity of components and interconnections but also by the density of the layout. A layout designed within the minimum area can require much more time than would be required if the area were larger. The most difficult layouts are those designed within minimum areas and using only one layer. Multilayer designs are not the most difficult. Each additional layer provides alternate paths for routing interconnecting tracks. Multilayer designs do require the designer to draw many more pencil lines, but the time consumed in drawing those lines is much less than the time required to make the decision about where to draw them. To emphasize this point, consider that a layout might require two weeks to create yet might only require four hours to trace onto another piece of paper.

Another factor that can have a large influence on the time required to complete a layout is the additional time required if changes are made to the circuit after the layout design has begun. A change of only one interconnection (on the schematic) might require extensive revision to the layout. It is a rare case when no change is made. (Changes occur in spite of the circuits having been bread-boarded.) Therefore time estimates should include approximately 25% additional time to incorporate changes.

1.7 (Cont.) LEAD TIME

The time required to generate the large scale artwork is a direct function of the number of layers and the complexity of each layer. Obviously, for a multilayer circuit, the artwork of a continuous plane of metallization requires far less time than a pattern of conductor tracks.

The delivery of purchased parts has often been the pacing factor in the lead time for producing prototypes. For this reason it is a good practice to select alternate components whenever possible and to indicate these alternatives on the parts list. Changes to the circuit can also have a large impact on the delivery of purchased parts.

1.8 PACKAGING DENSITY

Not only the layout designer but also the circuit design engineer should have some guidelines for approximating the size required to package a particular circuit using hybrid techniques.

If the size determination is delayed until the layout design is completed, then any changes that might be required to the partitioning can have far greater impact, since many commitments may have already been made.

The only known quantitative ground rules for determining package size do indicate the package size but are not definitive about the requirements for interconnecting tracks.

The given multiplication factors when applied to the individual component areas provide sufficient surface area for component mounting pads, wire bonding pads, and area for routing a relatively simple interconnecting pattern. Complex interconnections are not included.

SUBSTRATE AREA GROUND RULE

To determine the substrate area required to comfortably accommodate a particular circuit, multiply the area of each circuit component by the factor shown. The sum of these individually multiplied areas will provide for components, wire bonds and some additional area for interconnecting tracks. Because there is extra allowance in the multiplication factors, the calculated total area has proven to be comfortably large. Eighty percent of the calculated area should be treated as the minimum required.

1.8 (Cont.) PACKAGING DENSITY

<u>Component</u>	<u>Multiplication Factor</u>
Integrated Circuit	10 x
Transistor	4 x
Diode	3 x
Resistor	3 x
Capacitor	2 x
Inductor	2 x

NOTE: For any component size less than 50 x 50 mils, assume 50 x 50 mils, then apply multiplication factor.

Interconnect requirements are unique for each circuit and vary over a wide range of complexities. In some cases, where the interconnections are very simple or very few, they might be accommodated within the multiplication factors. Sometimes, however, even simple interconnections require the use of a few surface-to-surface jumpers in order to avoid multiple layers.

The number of layers required for interconnecting tracks is determined by several factors. Some of those factors are: the number of connections, the number of points to be connected on any one "string", whether or not the signals are preassigned to certain package leads, and very significant is whether components can be mounted on the top layer or must be directly on the substrate surface. There is no known groundrule that takes into account all of the variables in relation to each other.

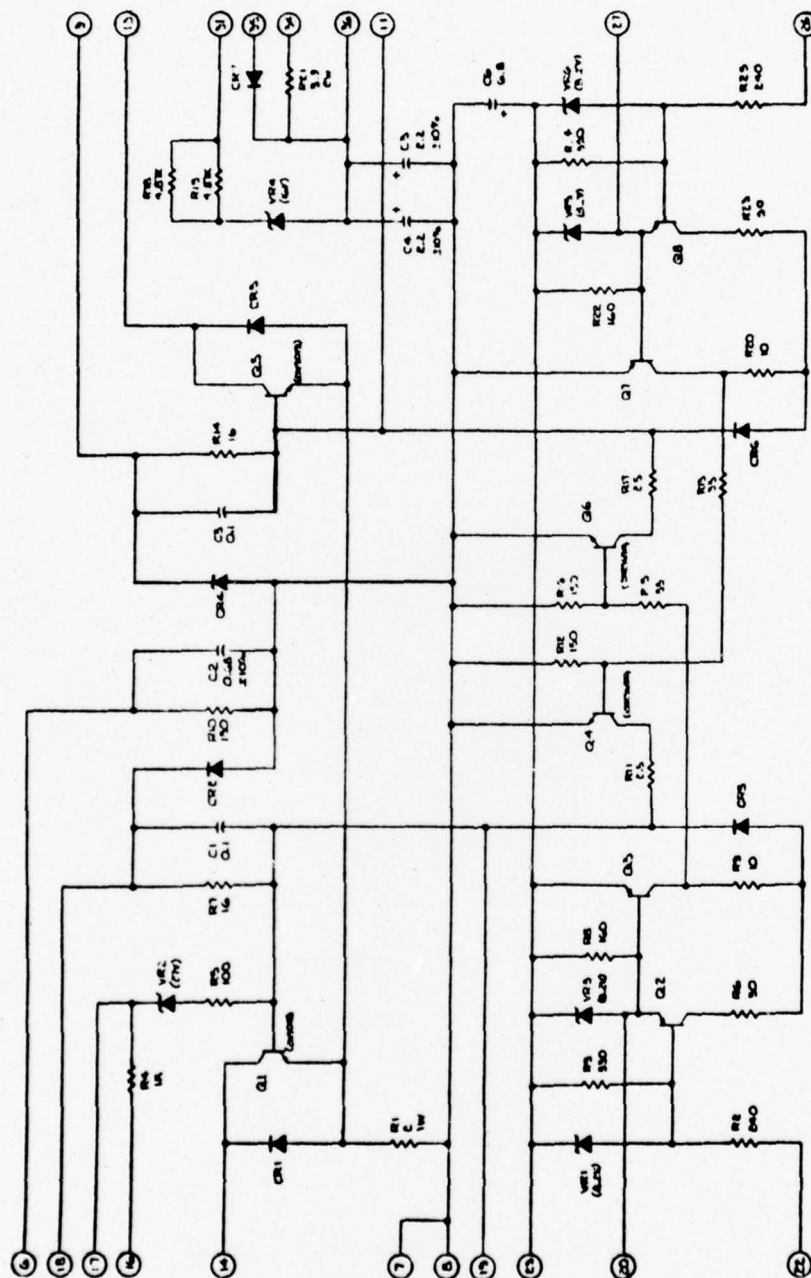
1.8 (Cont.) PACKAGING DENSITY

The substrate area groundrule, as previously stated, provides for some of the variables. The rule was applied on one project requiring eighty-six unique microcircuits. The designs incorporated flying wire bonds which were permitted to pass over surface conductor tracks up to a maximum wire length of 100 mils. All resistors were chips. Ten mil lines and spaces were the minimums used. None of the package pins were preassigned.

The following circuits along with their microcircuit designs are offered as examples of various circuit complexities. The schematic diagram is shown in order to depict the degree of complexity of the interconnections. A chart is provided which shows the application of the substrate area groundrule. The assembly picture and the metallization patterns make clear the density of the completed design.

1.8 (Cont.) PACKAGING DENSITY

Circuit No. 1 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 1 substrate area calculation:

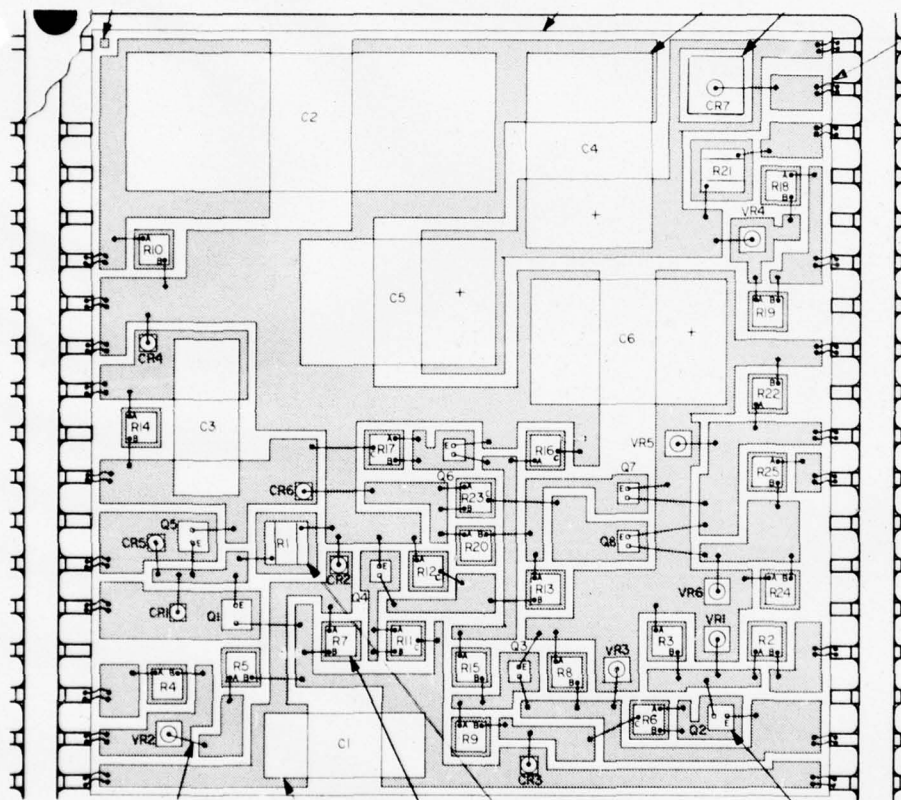
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x				
C1, 3	0.075 x 0.175 (1.90 x 4.44)	0.0131 (8.452)	0.0262 (16.903)	0.0524 (33.806)
C2	0.160 x 0.425 (4.06 x 10.79)	0.0680 (43.871)	0.0680 (43.871)	0.1360 (87.742)
C4, 5, 6	0.225 x 0.145 (5.71 x 3.68)	0.0326 (21.032)	0.0978 (63.097)	0.1956 (126.193)
Diodes: 3x				
CR1 thru 6	0.020 x 0.020 ¹ (0.51 x 0.51)	0.0025 (1.613)	0.0150 (9.677)	0.0450 (29.032)
CR7	0.060 x 0.060 (1.52 x 1.52)	0.0036 (2.322)	0.0036 (2.322)	0.0108 (6.968)
VR1 thru 6	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0025 (1.613)	0.0150 (9.677)	0.0450 (29.032)
Resistors: 3x				
R2 thru 20 } R22 thru 25 }	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0025 (1.613)	0.0575 (37.097)	0.1725 (111.290)
R1, 21	0.050 x 0.050 (1.27 x 1.27)	0.0025 (1.613)	0.0050 (3.226)	0.0150 (9.677)
Transistors: 4x				
Q1, 5	0.035 x 0.035 ¹ (0.89 x 0.89)	0.0025 (1.613)	0.0050 (3.226)	0.0200 (12.903)
Q2, 3, 4, 6, } Q7, 8 }	0.025 x 0.025 ¹ (0.63 x 0.63)	0.0025 (1.613)	0.0150 (9.677)	0.0600 (38.710)
			Total =	0.7523 (485.354)
Actual Substrate Size	0.850 x 0.880 (21.59 x 22.35)	0.7480 (482.580)		

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 99% of calculated area.

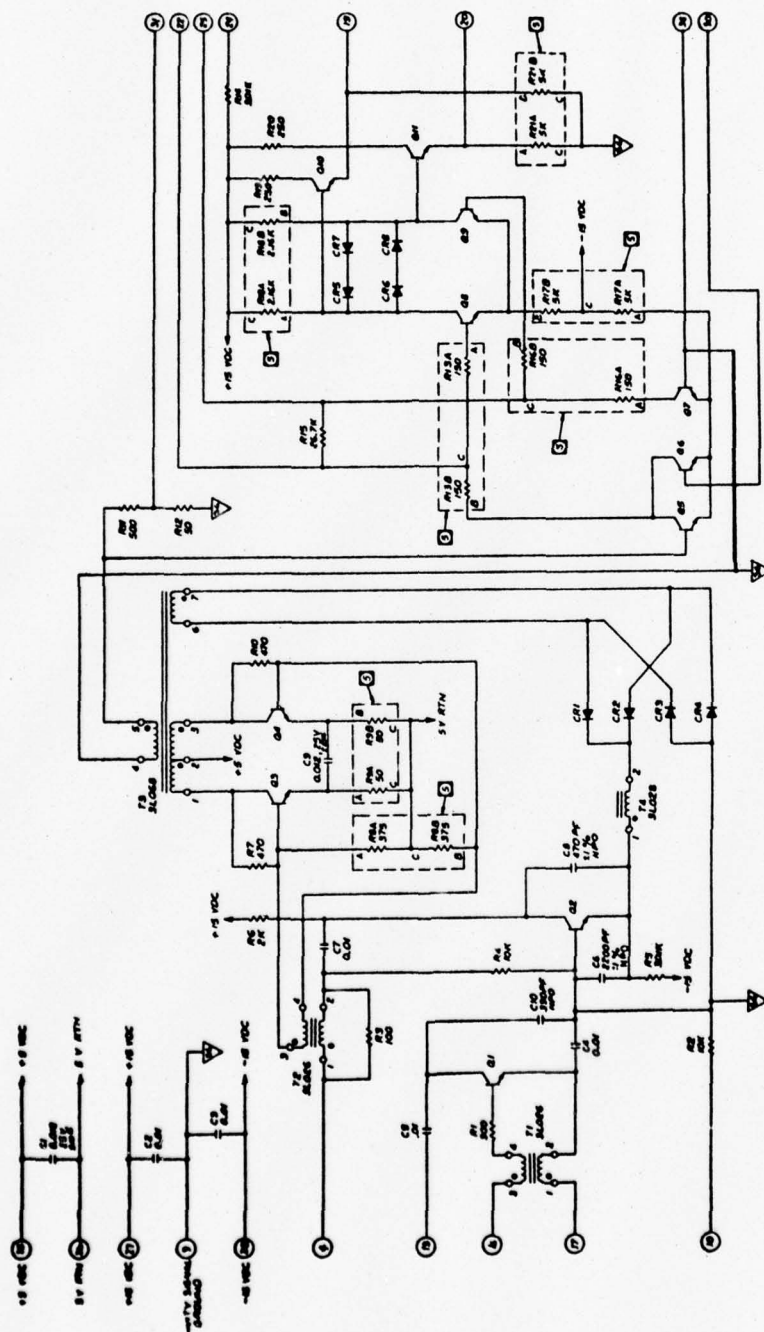
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 1 components plus single metallization layer:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 2 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 2 substrate area calculation:

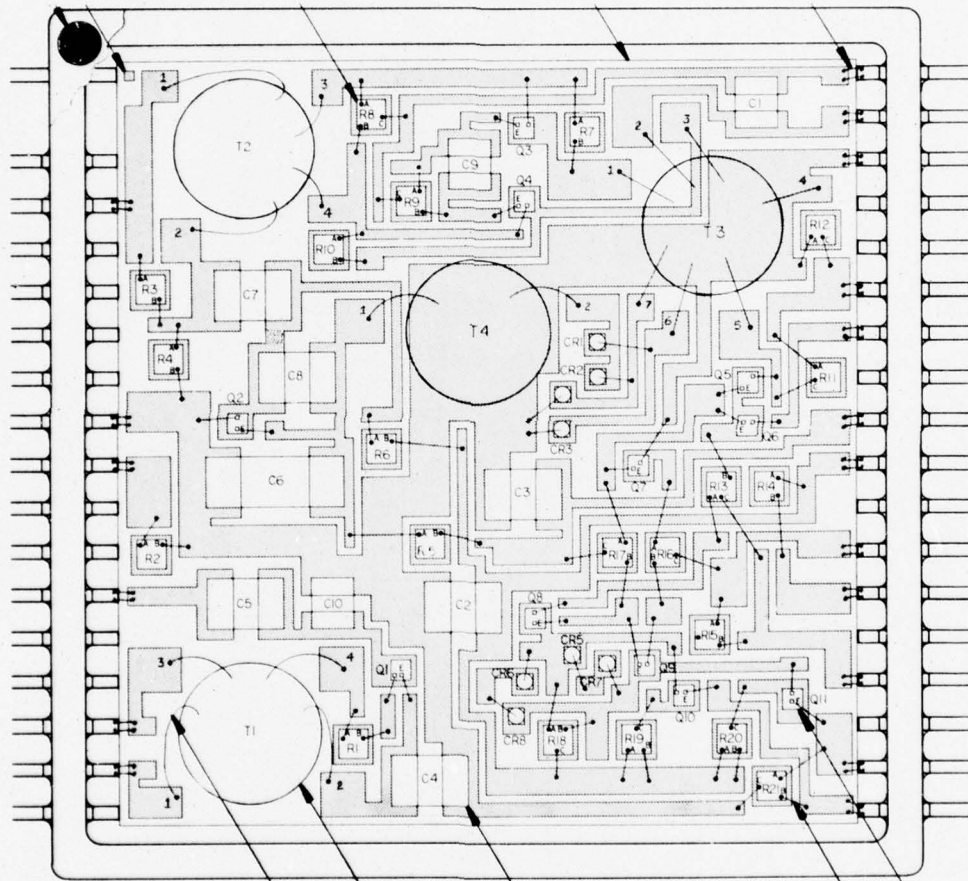
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total		Multiplied Area	
			sq in. (sq mm)	in. (mm)	sq in. (sq mm)	in. (mm)
Capacitors: 2x C1, 9, 10	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0090 (5.806)		0.0180 (11.613)	
C2, 3, 4, 5, } C7, 8	0.060 x 0.090 (1.52 x 2.29)	0.0054 (3.484)	0.0324 (20.903)		0.0648 (41.806)	
C6	0.060 x 0.160 (1.52 x 4.06)	0.0096 (6.193)	0.0096 (6.193)		0.0192 (12.387)	
Diodes: 3x CR1 thru 8	¹ 0.020 x 0.020 (0.51 x 0.51)	0.0025 (1.613)	0.0200 (12.903)		0.0600 (38.710)	
Resistors: 3x R1 thru 20	¹ 0.030 x 0.030 (0.76 x 0.76)	0.0025 (1.613)	0.0500 (32.258)		0.1500 (96.774)	
Transistors: 4x Q1 thru 11	¹ 0.025 x 0.025 (0.63 x 0.63)	0.0025 (1.613)	0.0275 (17.742)		0.1100 (70.968)	
Toroids: 2x T1 thru 4	0.160 Dia (4.06)	0.020 (12.903)	0.080 (51.613)		0.160 (103.226)	
			Total =		0.582 (375.483)	
Actual Substrate size	0.850 x 0.880 (21.59 x 22.35)	0.748 (482.580)				

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 128% of calculated area.

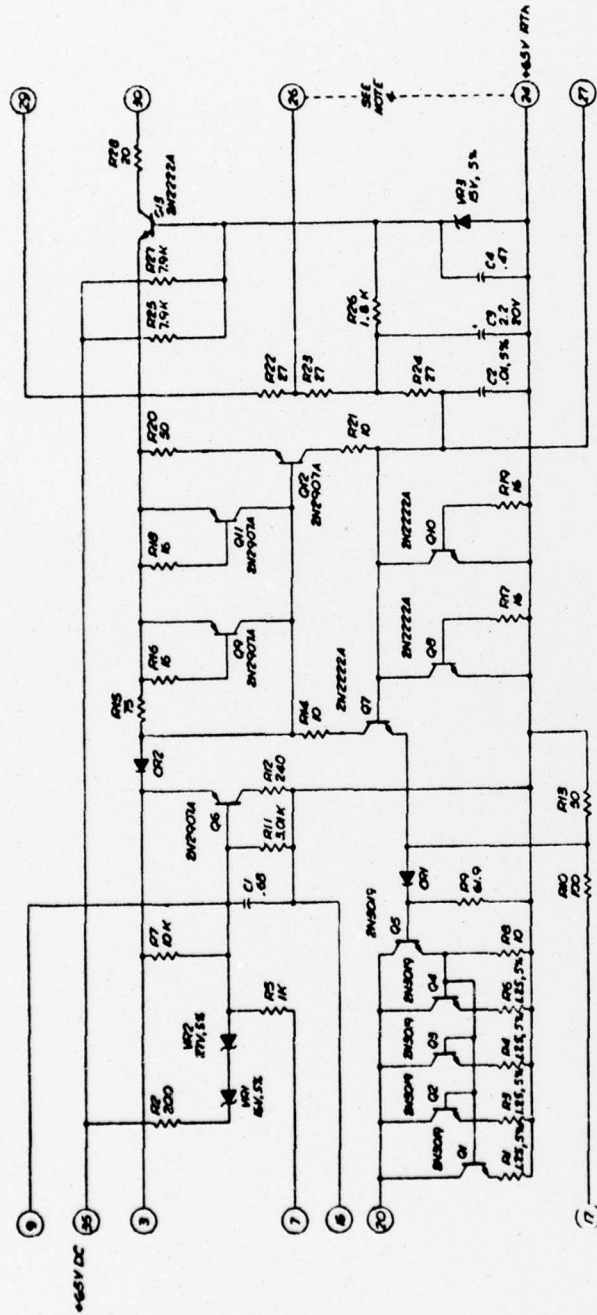
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 2, components plus single metallization layer:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 3 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 3 substrate area calculation:

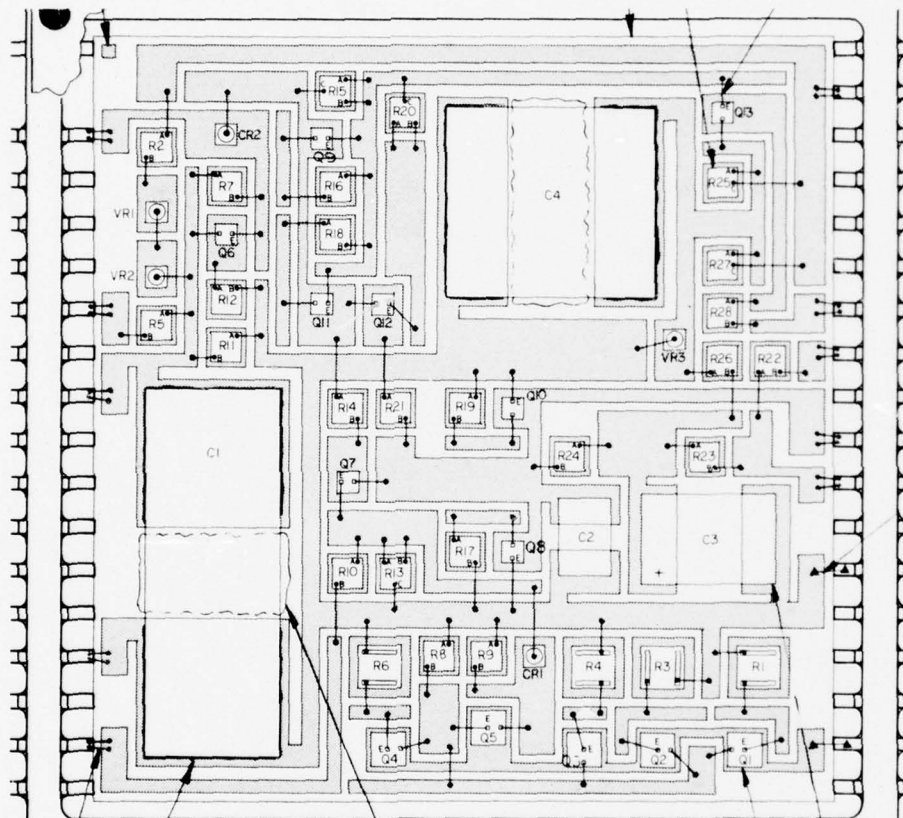
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x				
C1	0.155 x 0.325 (3.94 x 8.25)	0.0504 (32.516)	0.0504 (32.516)	0.1008 (65.032)
C2	0.060 x 0.090 (1.52 x 2.29)	0.0054 (3.484)	0.0054 (3.484)	0.0108 (6.968)
C3	0.105 x 0.155 (2.67 x 3.94)	0.0163 (10.516)	0.0163 (10.516)	0.0326 (21.032)
C4	0.220 x 0.240 (5.59 x 6.10)	0.0528 (34.064)	0.0528 (34.064)	0.1056 (68.129)
Diodes: 3x				
CR1, 2 VR1, 2, 3 }	0.025 x 0.025 ¹ (0.63 x 0.63)	0.0025 (1.613)	0.0125 (8.064)	0.0375 (24.193)
Transistors: 4x				
Q1 thru 5	0.040 x 0.040 ¹ (1.02 x 1.02)	0.0025 (1.613)	0.0125 (8.064)	0.0500 (32.258)
Q6 thru 13	0.025 x 0.025 ¹ (0.63 x 0.63)	0.0025 (1.613)	0.0200 (12.903)	0.0800 (51.613)
Resistors: 3x				
R1, 3, 4, 6	0.050 x 0.050 (1.27 x 1.27)	0.0025 (1.613)	0.0100 (6.452)	0.0300 (19.355)
R2, 5 R7 thru 28 }	0.035 x 0.035 ¹ (0.89 x 0.89)	0.0025 (1.613)	0.0600 (38.710)	0.1800 (116.129)
			Total =	0.627 (404.709)
Actual Substrate Size	0.855 x 0.885 (21.72 x 22.48)	0.757 (488.176)		

¹ Sizes less than 0.050 x 0.050 in (1.27 x 1.27 mm) assume 0.050 x 0.050 in (1.27 x 1.27 mm).

Actual substrate size is 120% of calculated area.

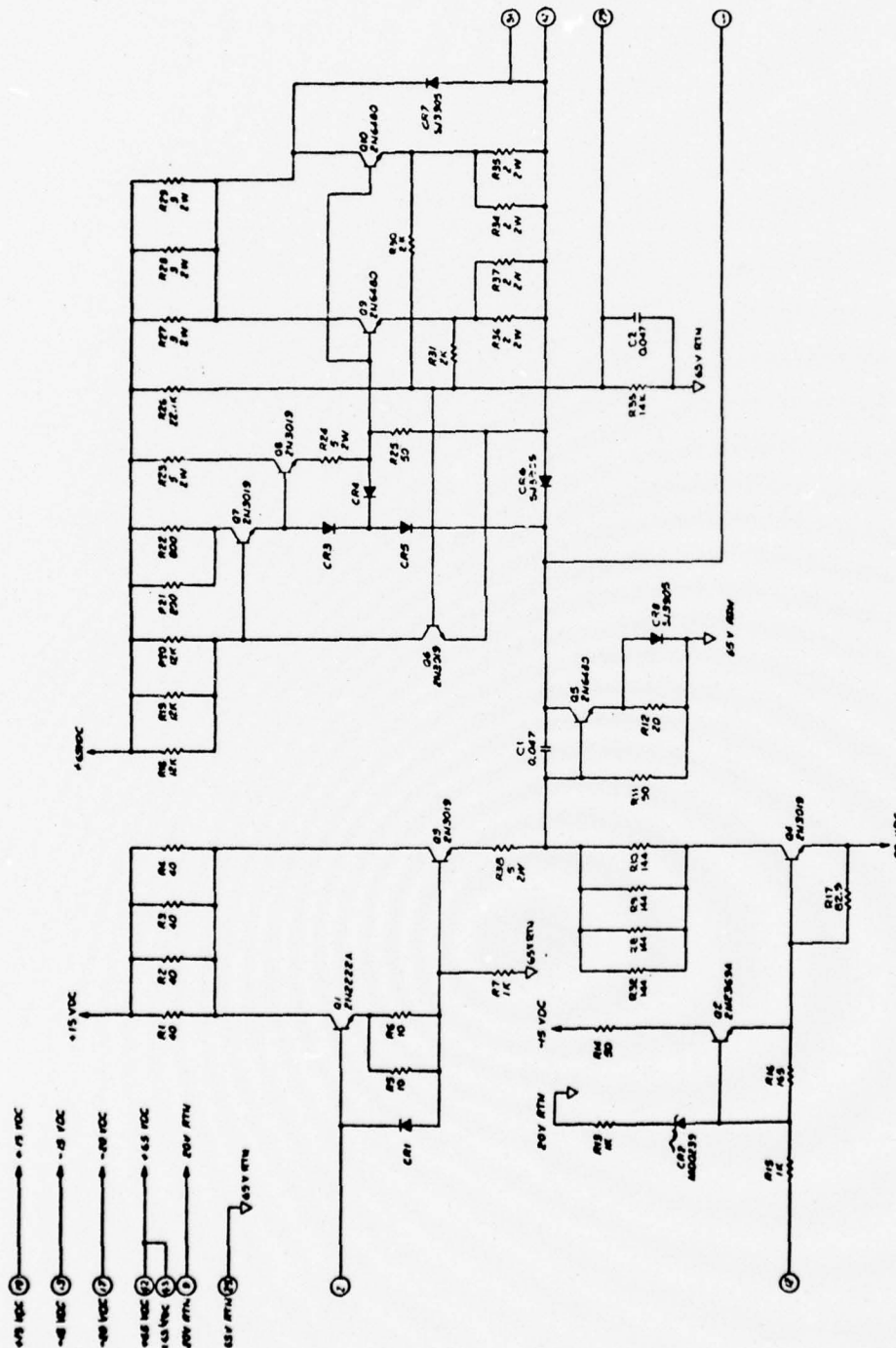
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 3, components plus single metallization layer:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 4 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 4 substrate area calculation:

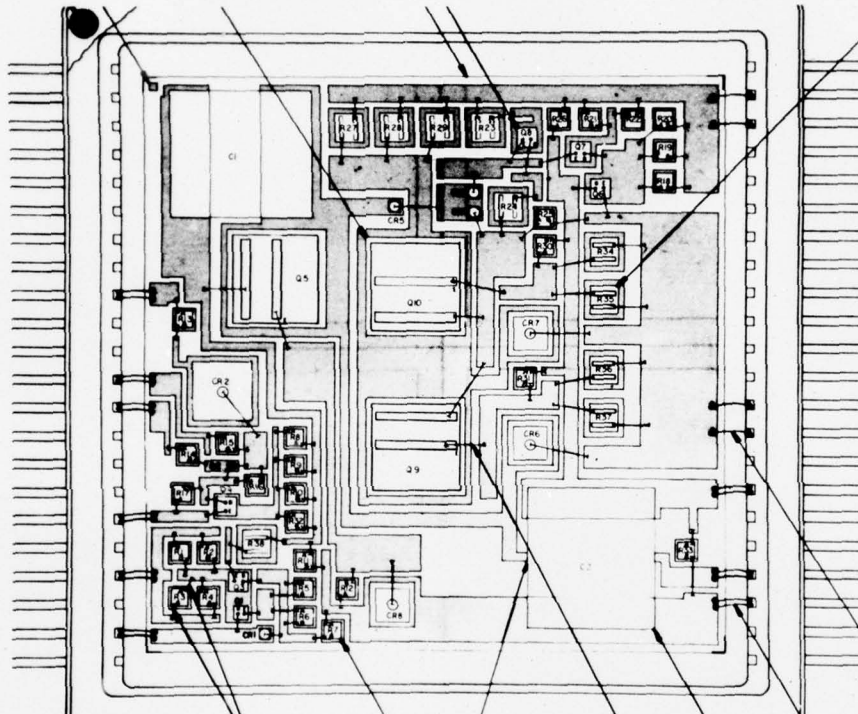
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x C1, 2	0.225 x 0.250 (5.71 x 6.35)	0.0562 (36.258)	0.1124 (72.516)	.225 (145.032)
Diodes: 3x CR1, 3, 4, 5	0.020 x 0.020 ^Δ (0.51 x 0.51)	0.0025 (1.613)	0.0100 (6.452)	0.0300 (19.355)
CR2	0.085 x 0.085 (2.16 x 2.16)	0.0072 (4.645)	0.0072 (4.645)	0.0216 (13.935)
CR6, 7, 8	0.060 x 0.060 (1.52 x 1.52)	0.0036 (2.322)	0.0108 (6.968)	0.0324 (20.903)
Transistors: 4x Q1	0.025 x 0.025 ^Δ (0.63 x 0.63)	0.0025 (1.613)	0.0025 (1.613)	0.0100 (6.452)
Q2	0.010 x 0.015 ^Δ (0.25 x 0.38)	0.0025 (1.613)	0.0025 (1.613)	0.0100 (6.452)
Q3, 4, 6, 7, Q8	0.035 x 0.035 ^Δ (0.89 x 0.89)	0.0025 (1.613)	0.0125 (8.065)	0.0500 (32.258)
Q5, 9, 10	0.175 x 0.175 (4.44 x 4.44)	0.0306 (19.742)	0.0919 (59.290)	0.3676 (237.161)
Resistors: 3x R1 thru 22, } R25, 26, } R30 thru 33 }	0.030 x 0.030 ^Δ (0.76 x 0.76)	.0025 (1.613)	0.0700 (45.161)	0.2100 (135.484)
R23, 24, 27, } R28, 29, 34, } R35, 36, 37, } R38	0.050 x 0.050 (1.27 x 1.27)	.0025 (1.613)	0.0250 (16.129)	0.0750 (48.387)
			Total =	1.0316 (665.547)
Actual Substrate Size	1.020 x 1.020 (25.91 x 25.91)	1.0404 (671.224)		

^Δ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 100%+ of the calculated area.

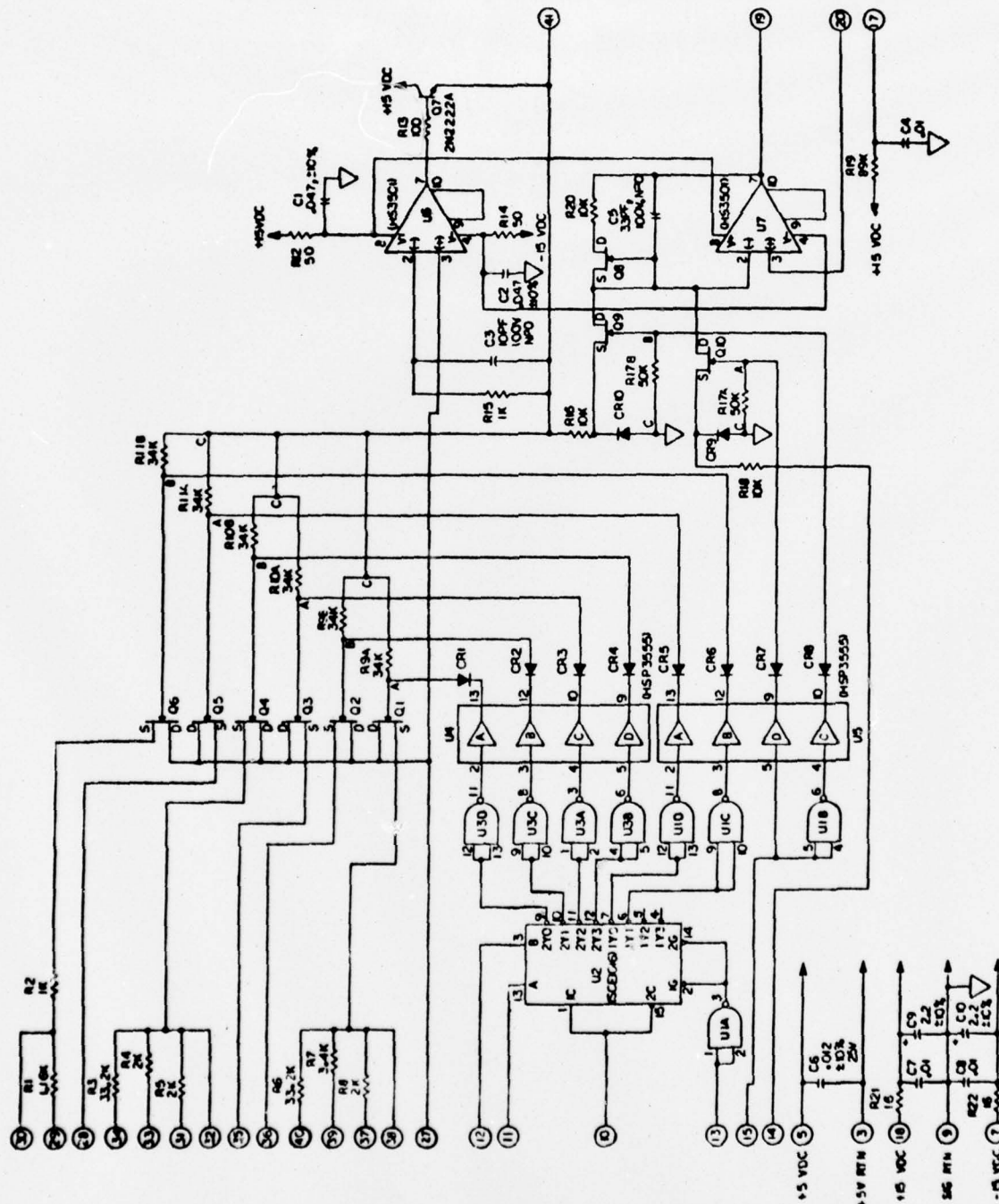
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 4, components plus single metallization layer:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 5 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 5 substrate area calculation:

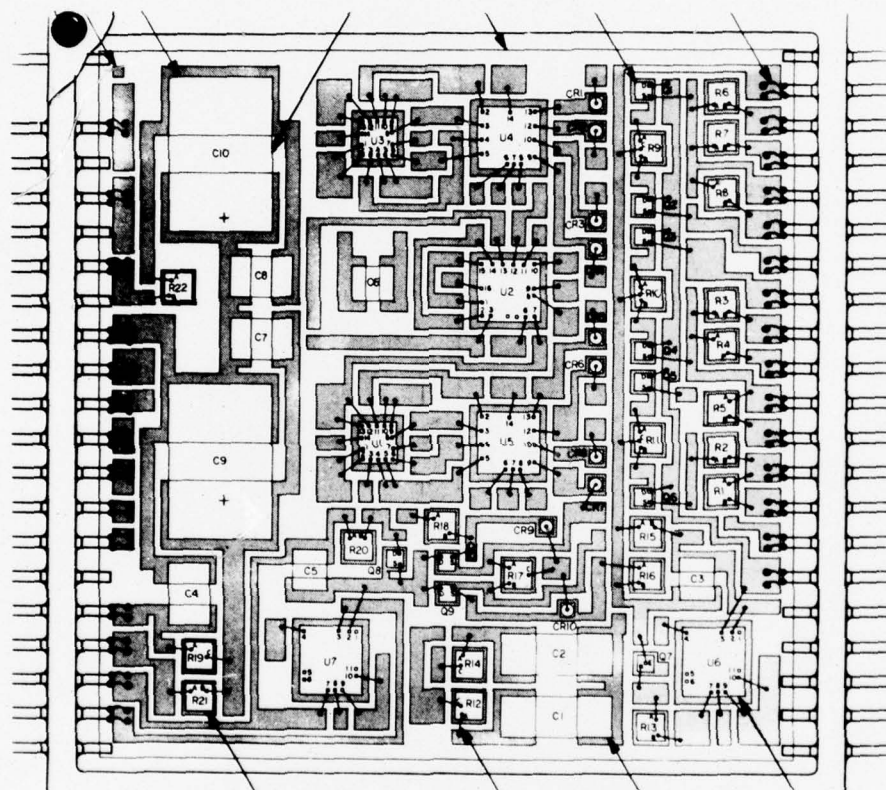
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x C1, 2	0.060 x 0.155 (1.52 x 3.94)	0.0093 (6.000)	0.0186 (12.000)	0.0372 (24.000)
C3, 5	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0060 (3.871)	0.0120 (7.742)
C4, 7, 8	0.060 x 0.090 (1.52 x 2.29)	0.0054 (3.484)	0.0162 (10.452)	0.0324 (20.903)
C6	0.065 x 0.060 (1.65 x 1.52)	0.0039 (2.516)	0.0039 (2.516)	0.0078 (5.032)
C9, 10	0.150 x 0.225 (3.81 x 5.71)	0.0337 (21.742)	0.0675 (43.548)	0.1350 (87.097)
Diodes: 3x CR1 thru 10	0.020 x 0.020 ¹ (0.51 x 0.51)	0.0025 (1.613)	0.0250 (16.129)	0.0750 (48.387)
Resistors: 3x R1 thru 22	0.040 x 0.040 ¹ (1.02 x 1.02)	0.0025 (1.613)	0.550 (35.484)	0.1650 (106.451)
Transistors: 4x Q1 thru 10	0.025 x 0.025 ¹ (0.63 x 0.63)	0.0025 (1.613)	0.0250 (16.129)	0.1000 (64.516)
I.C.'s: 10x U1, 3	0.055 x 0.060 (1.39 x 1.52)	0.0033 (2.129)	0.0066 (4.258)	0.0660 (42.580)
U2, 4, 5	0.090 x 0.090 (2.29 x 2.29)	0.0081 (5.226)	0.0243 (15.677)	0.2430 (156.770)
			Total =	1.0534 (679.612)
Actual Substrate Size	1.000 x 1.025 (25.40 x 26.03)	1.0250 (661.289)		

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 97% of the calculated area.

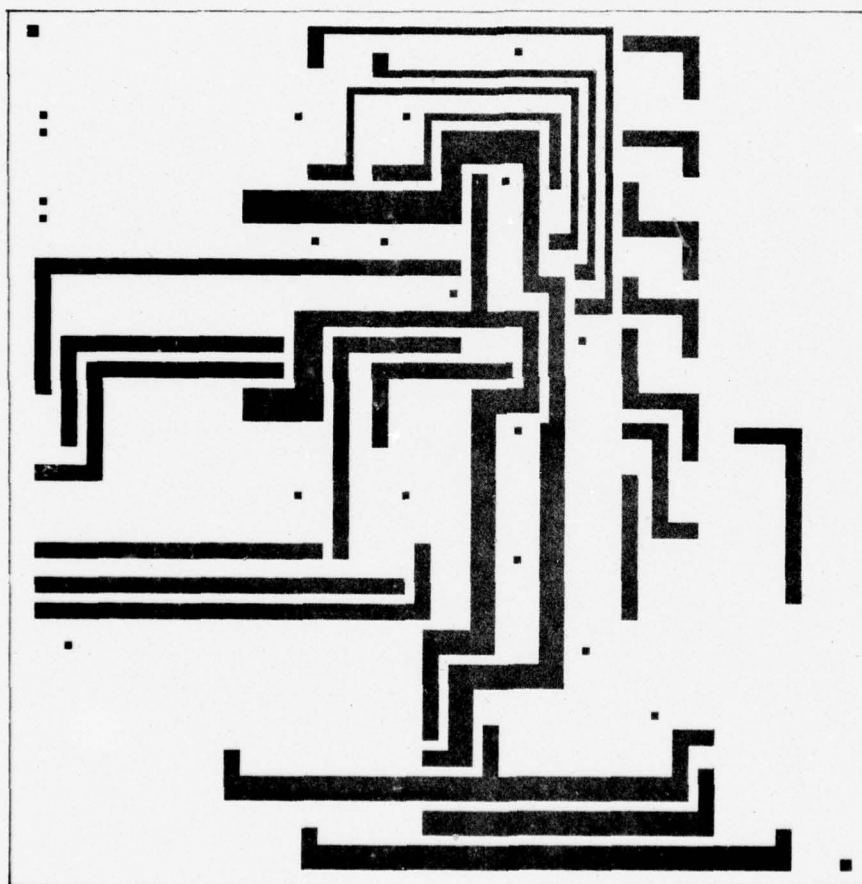
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 5, components plus 3rd metallization layer:



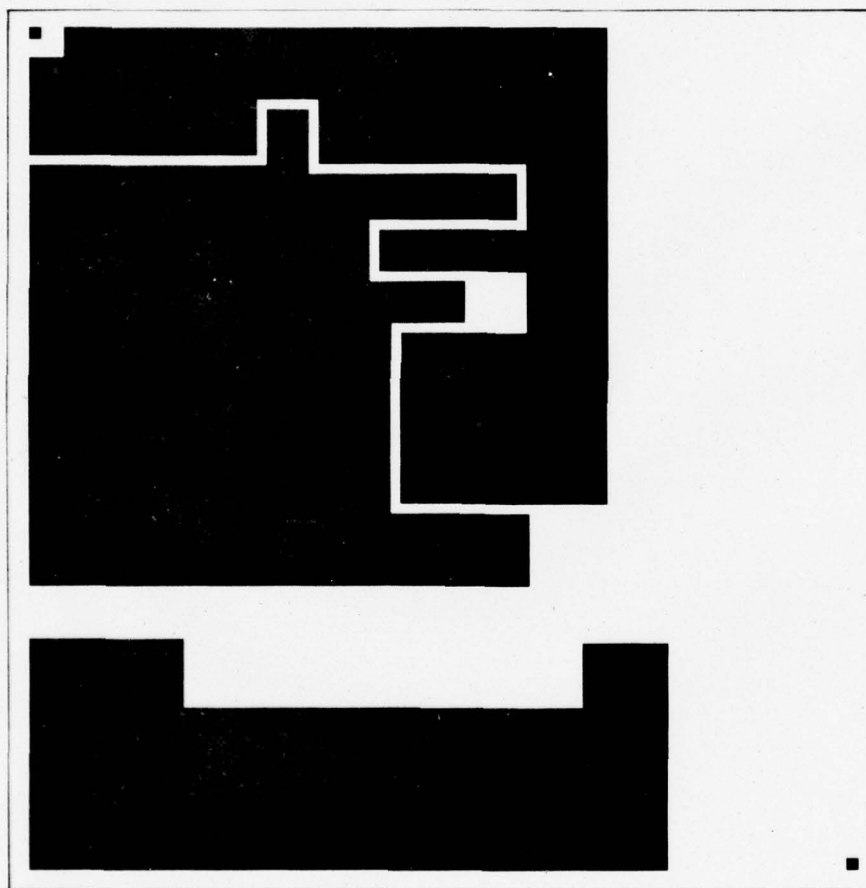
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 5, 2nd metallization layer (signal interconnections):



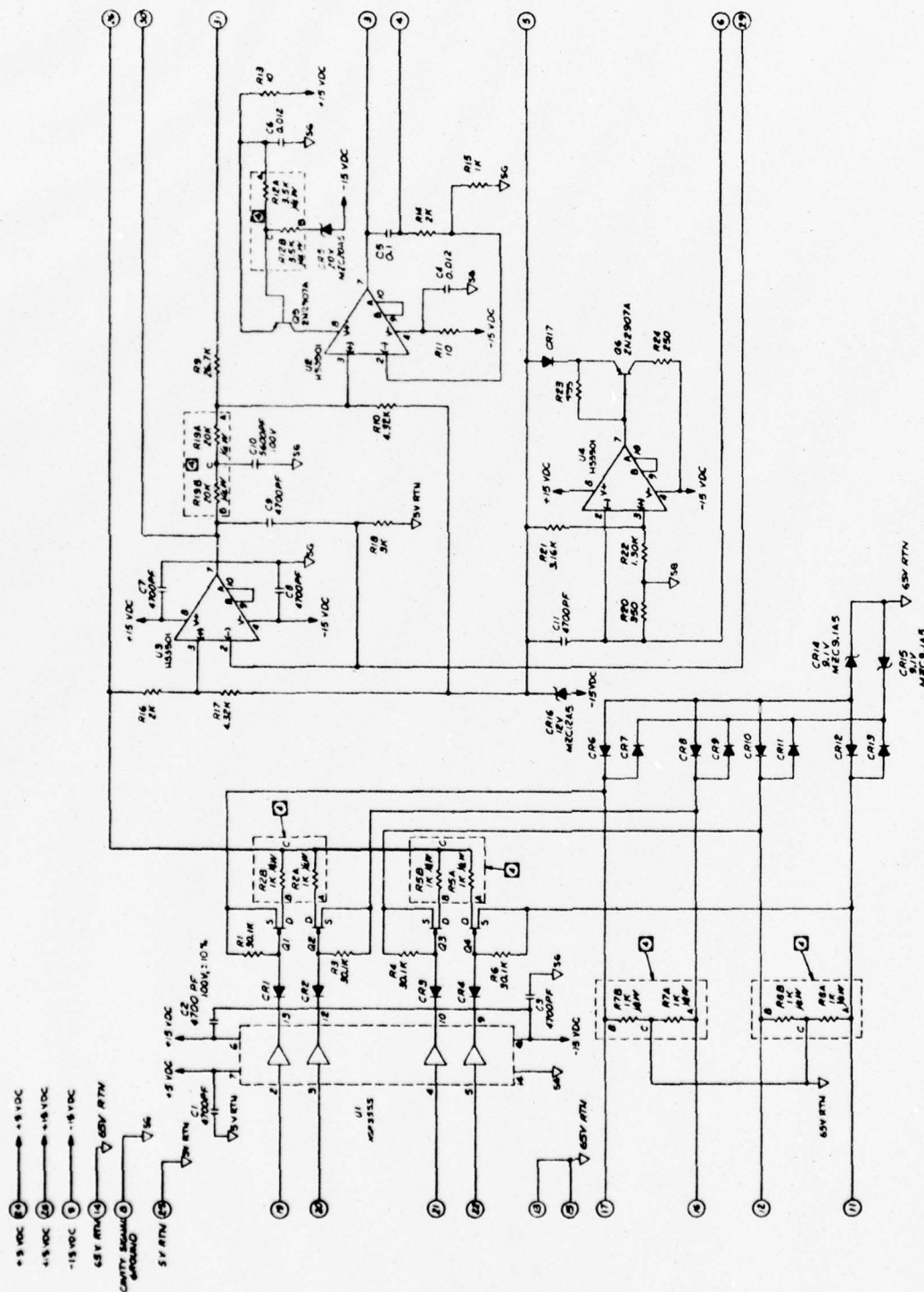
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 5, 1st metallization layer (GND and voltage connections):



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 6 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 6 substrate area calculation:

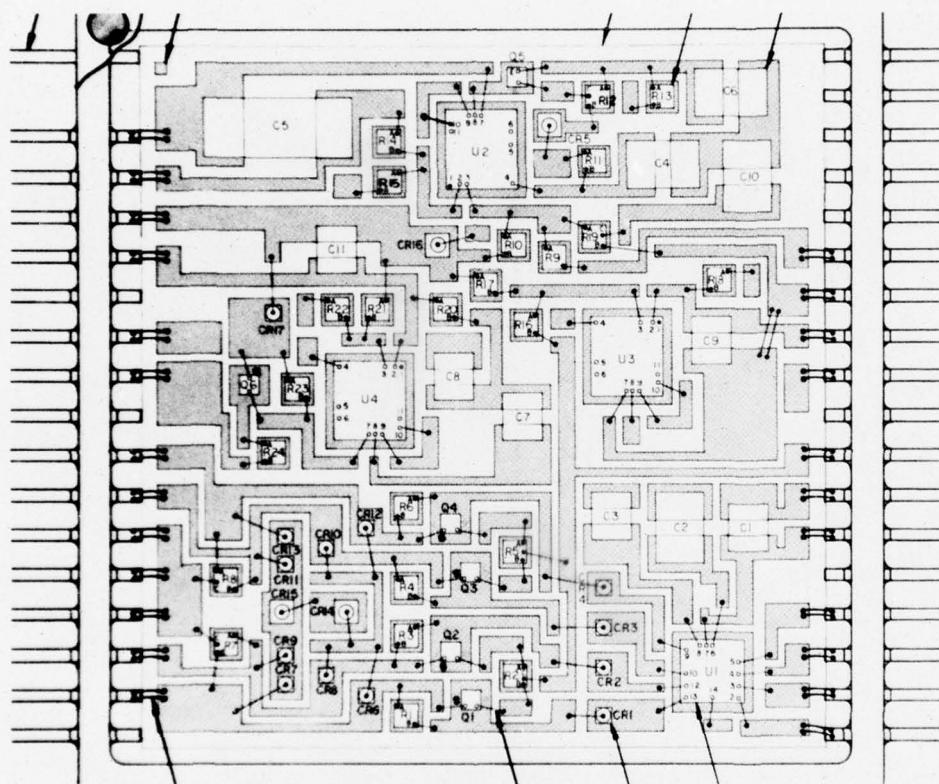
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x C1, 3, 7, 8, } C9, 11 }	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0180 (11.613)	0.0360 (23.226)
C2, 4, 6, 10	0.060 x 0.090 (1.52 x 2.29)	0.0054 (3.484)	0.0216 (13.935)	0.0432 (27.871)
C5	0.075 x 0.185 (1.90 x 4.70)	0.0139 (8.967)	0.0139 (8.967)	0.0278 (17.935)
Diodes: 3x CR1 thru 4, } C6 thru 13 } CR 17 }	0.020 x 0.020 ¹ (0.51 x 0.51)	0.0025 (1.613)	0.0325 (20.967)	0.0975 (62.993)
CR5, 14, 15, } CR16 }	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0025 (1.613)	0.0100 (6.452)	0.0300 (19.355)
Transistors: 4x Q1 thru 6	0.025 x 0.025 ¹ (0.63 x 0.63)	0.0025 (1.613)	0.0150 (9.677)	0.0600 (38.710)
Resistors: 3x R1 thru 24	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0025 (1.613)	0.0600 (38.710)	0.1800 (116.129)
I.C.'s: 10x U1	0.080 x 0.080 (2.03 x 2.03)	0.0064 (4.129)	0.0064 (4.129)	0.0640 (41.290)
U2, 3, 4	0.090 x 0.100 (2.29 x 2.54)	0.0090 (5.806)	0.0270 (17.419)	0.2700 (174.190)
			Total =	0.8085 (521.612)
Actual Substrate Size	0.855 x 0.885 (21.72 x 22.48)	0.7566 (488.128)		

¹ Sizes less than .050 x .050 in. (1.27 x 1.27 mm) assume .050 x .050 in. (1.27 x 1.27 mm).

Actual substrate area is 93% of calculated area.

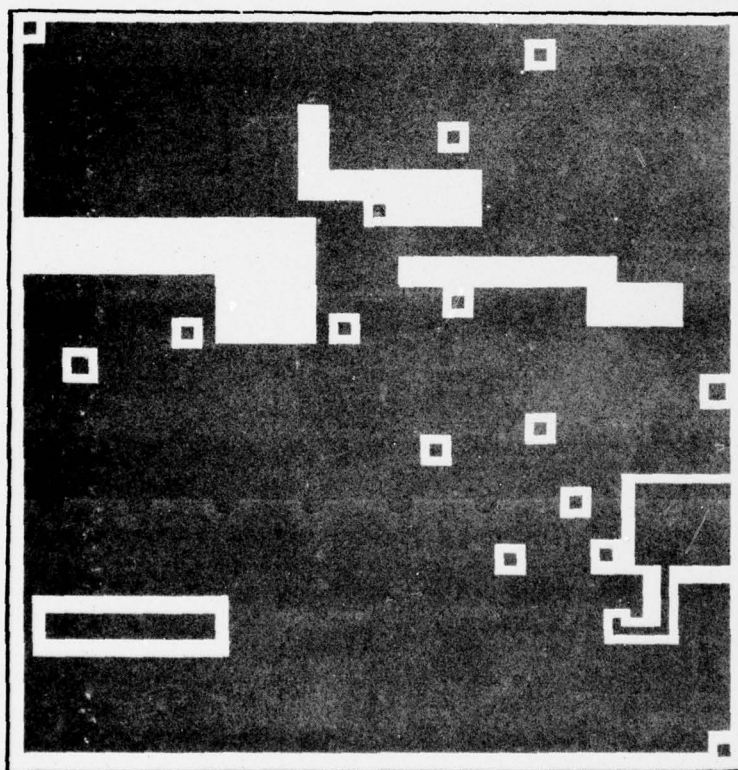
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 6, components plus 3rd metallization layer:



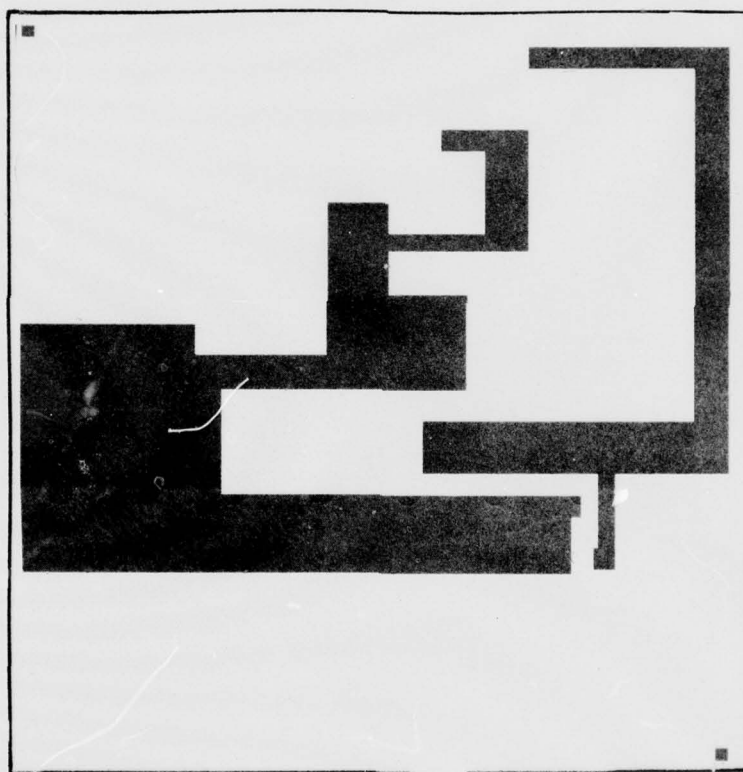
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 6, 2nd metallization layer (GND plane):



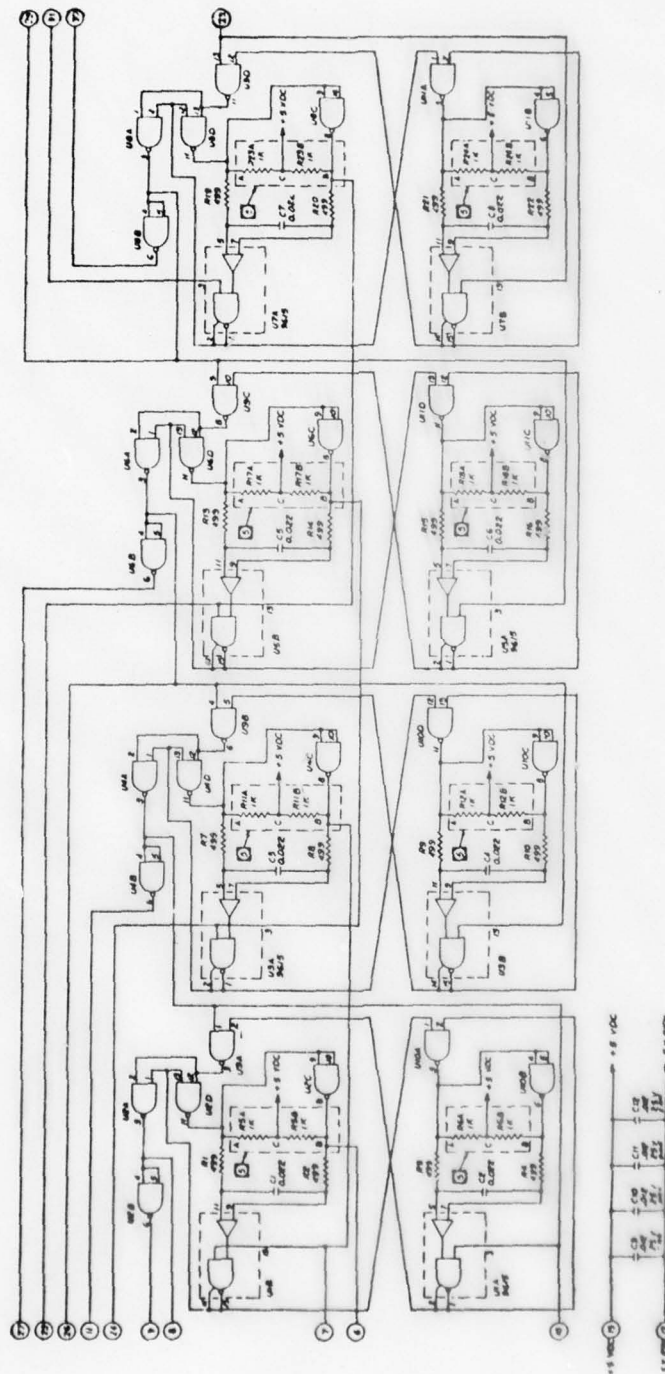
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 6, 1st metallization layer (voltage lines):



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7 substrate area calculation:

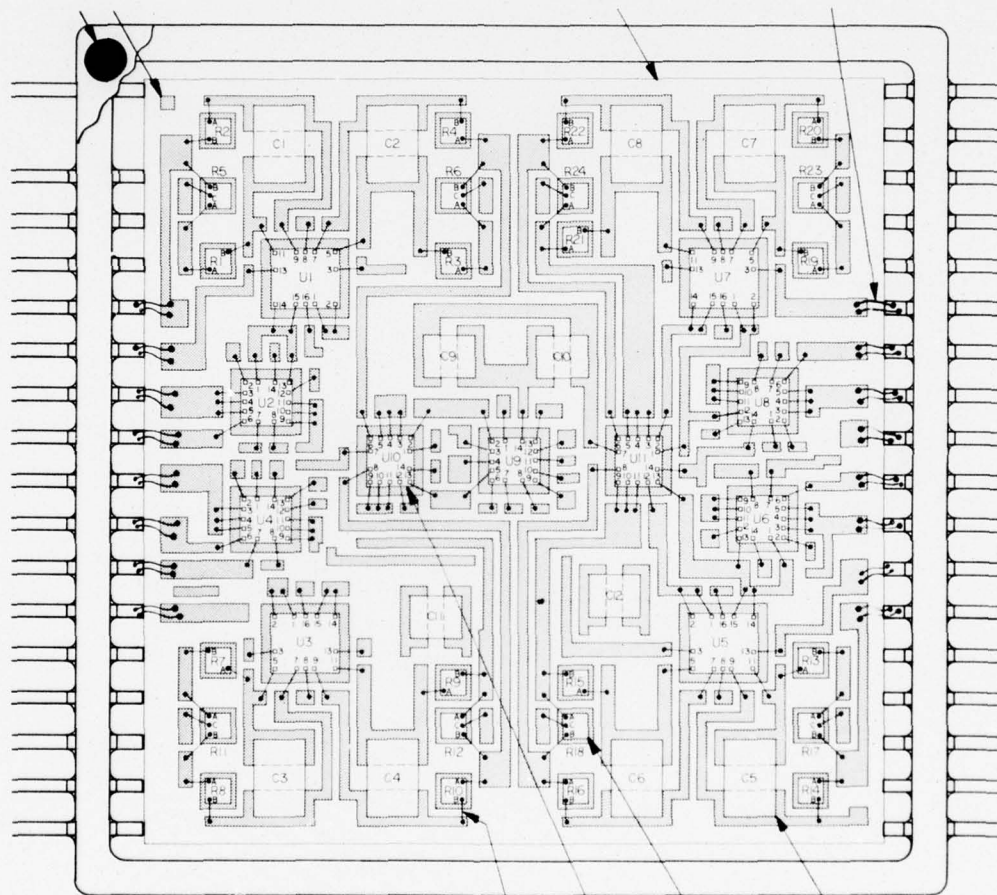
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq mm)	Multinplied Area sq in. (sq mm)
Capacitors: 2x C1 thru 8	0.060 x 0.090 (1.52 x 2.29)	0.0054 (3.484)	0.0432 (27.871)	0.0864 (55.742)
C9 thru 12	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0120 (7.742)	0.0240 (15.484)
Resistors: 3x R1 thru 24	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0009 (0.581)	0.0216 (13.935)	0.0648 (41.806)
I.C.'s: 10x U1, 3, 5, 7	0.080 x 0.070 (2.03 x 1.78)	.0056 (3.613)	0.0224 (14.451)	0.2240 (144.516)
U2, 4, 6, 8, U9, 10, 11	0.060 x 0.055 (1.52 x 1.40)	0.0033 (2.129)	0.0231 (14.903)	0.2310 (149.032)
			Total =	0.6302 (406.580)
Actual Substrate Size	0.850 x 0.880 (21.59 x 22.35)	0.7480 (482.580)		

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 118% of the calculated area.

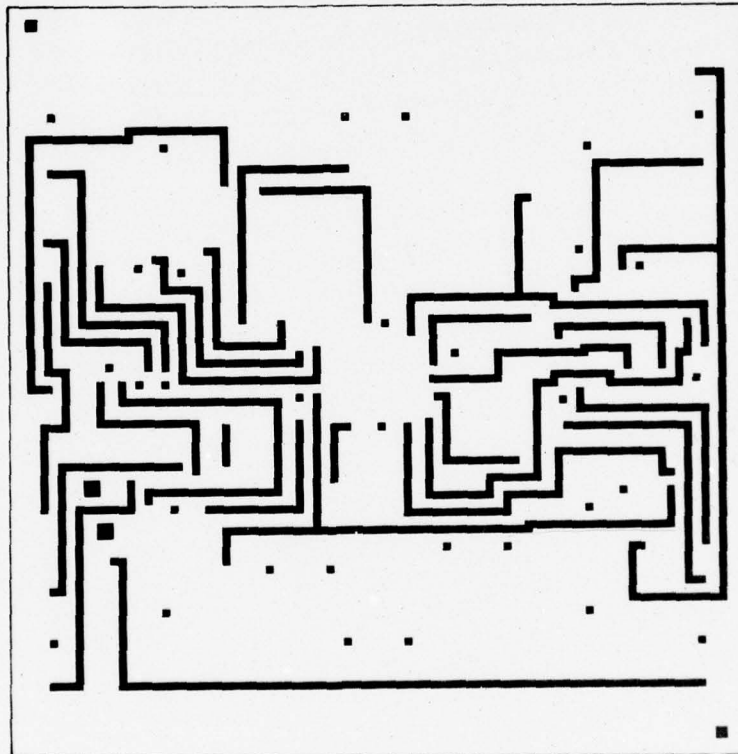
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7, components plus 4th metallization layer:



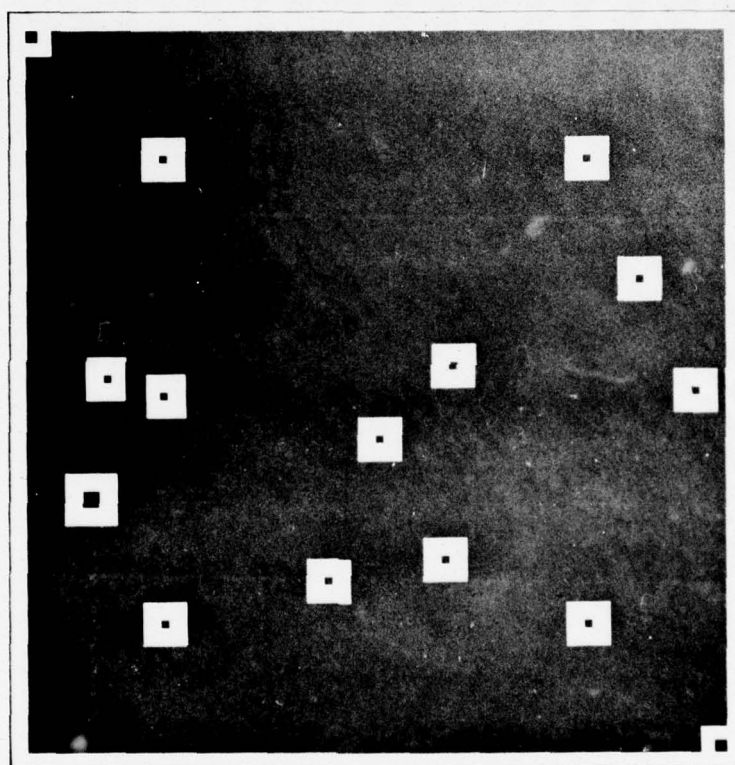
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7, 3rd metallization layer (signal interconnections):



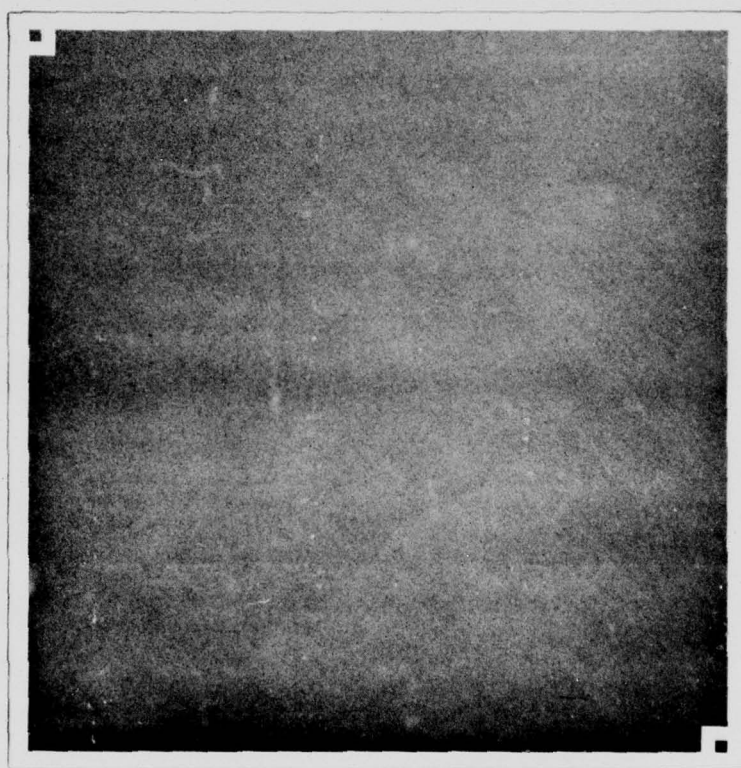
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7, 2nd metallization layer (voltage plane):

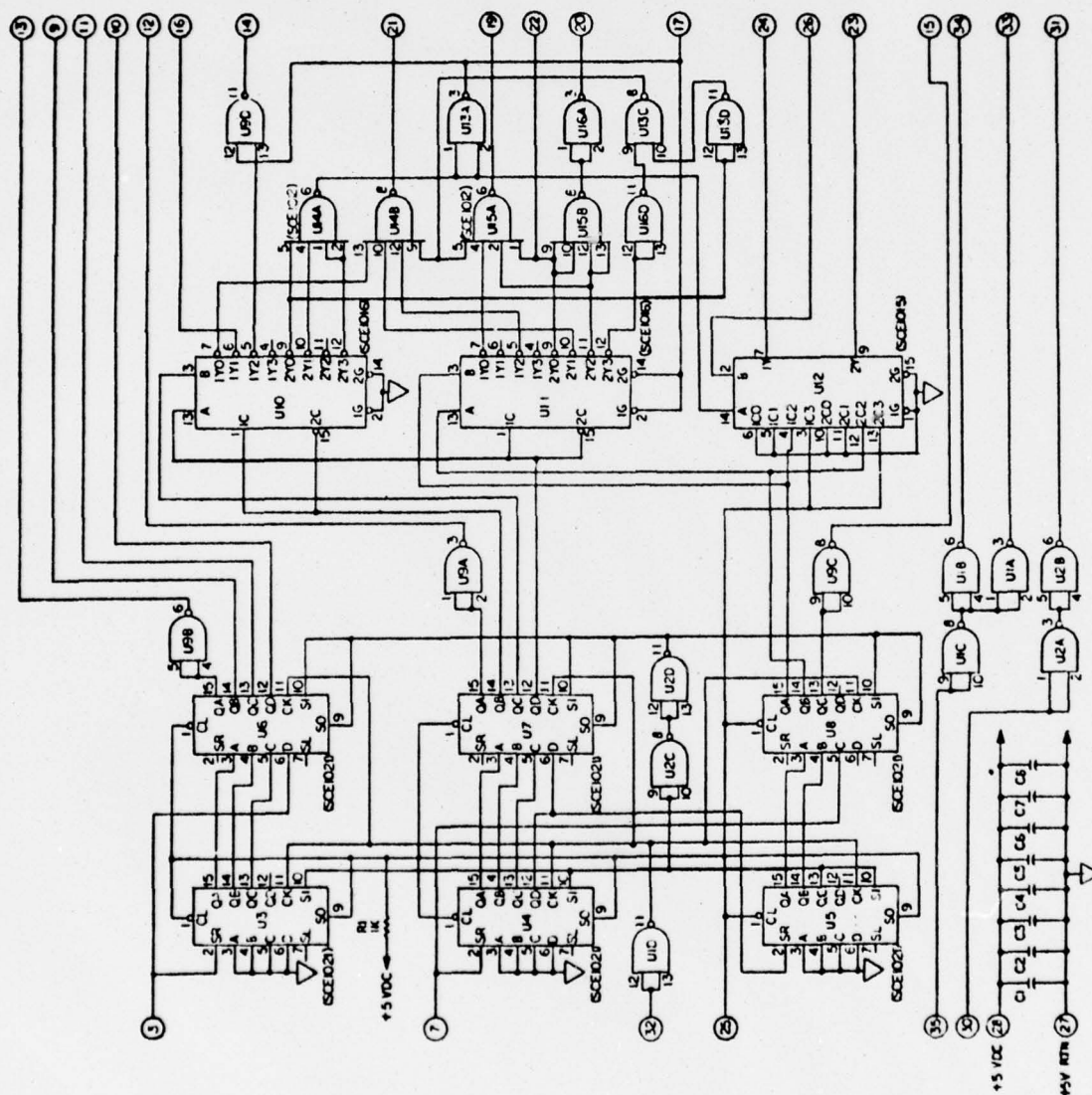


1.8 (Cont.) PACKAGING DENSITY

Circuit No. 7, 1st metallization layer (GND plane):



Circuit No. 8 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 8 substrate area calculation:

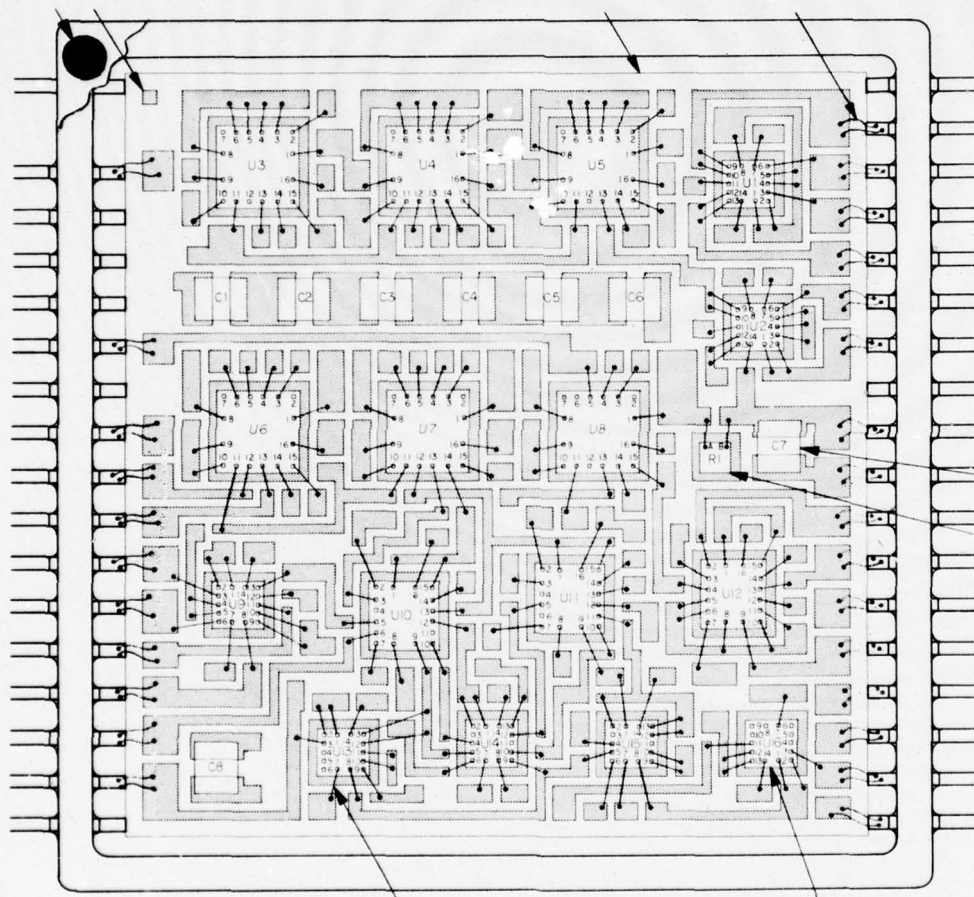
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total sq in. (sq. mm)	Multiplied Area sq in. (sq mm)
Capacitors: 2x C1 thru 8	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0240 (15.484)	0.0480 (30.968)
Resistors: 3x R1	0.030 x 0.030 ¹ (0.76 x 0.76)	0.0025 (1.613)	0.0025 (1.613)	0.0075 (4.839)
I.C.'s: 10x U1, 2, 9, 13, } U16	0.055 x 0.060 (1.40 x 1.52)	0.0033 (2.129)	0.0165 (10.645)	0.1650 (106.450)
U3 thru 8	0.095 x 0.095 (2.41 x 2.41)	0.0090 (5.806)	0.0540 (34.838)	0.5400 (348.380)
U10, 11	0.080 x 0.095 (2.03 x 2.41)	0.0076 (4.903)	0.0152 (9.806)	0.1520 (98.060)
U12	0.075 x 0.085 (1.90 x 2.16)	0.0064 (4.129)	0.0064 (4.129)	0.0640 (41.290)
U14, 15	0.055 x 0.060 (1.40 x 1.52)	0.0033 (2.129)	0.0066 (4.258)	0.0660 (42.580)
			Total =	1.0425 (672.579)
Actual Substrate Size	0.850 x 0.880 (21.59 x 22.35)	0.748 (482.580)		

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 72% of the calculated area. The smaller-than-80% substrate was not predicted before the design was initiated. Only after the first design was completed (on a larger size substrate) was it determined that an attempt should be made to use a smaller substrate.

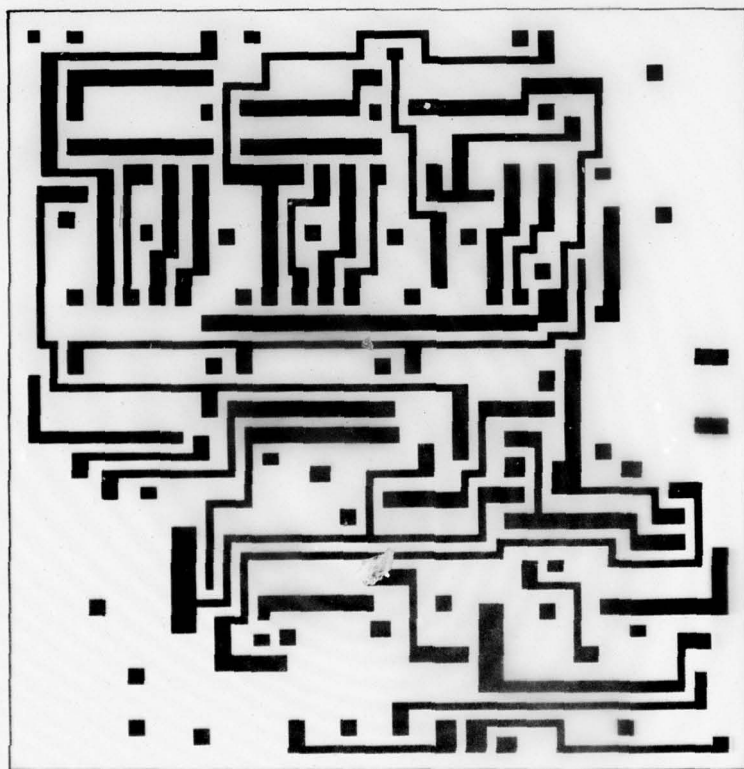
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 8 components plus 4th metallization layer:



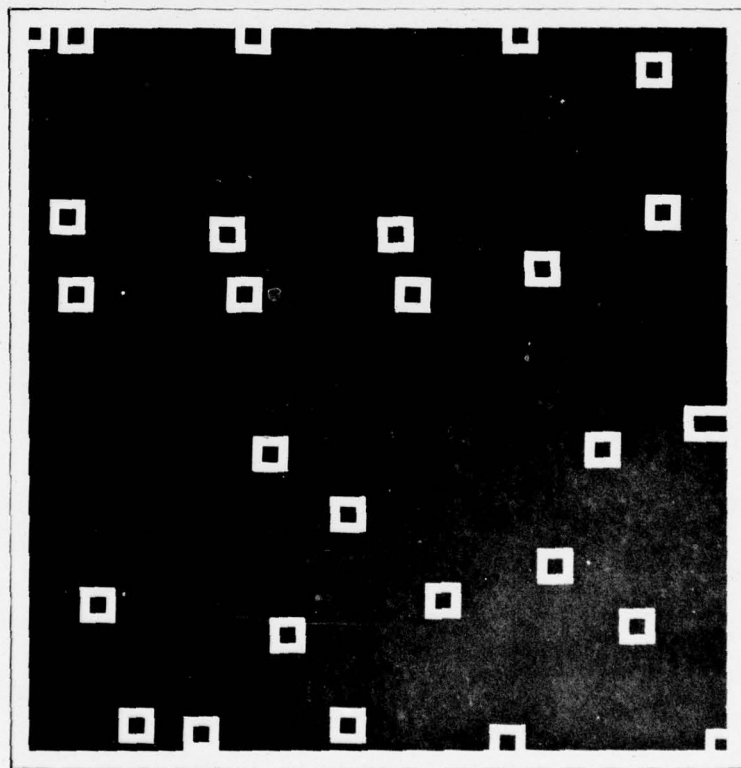
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 8, 3rd metallization layer (signal interconnections):



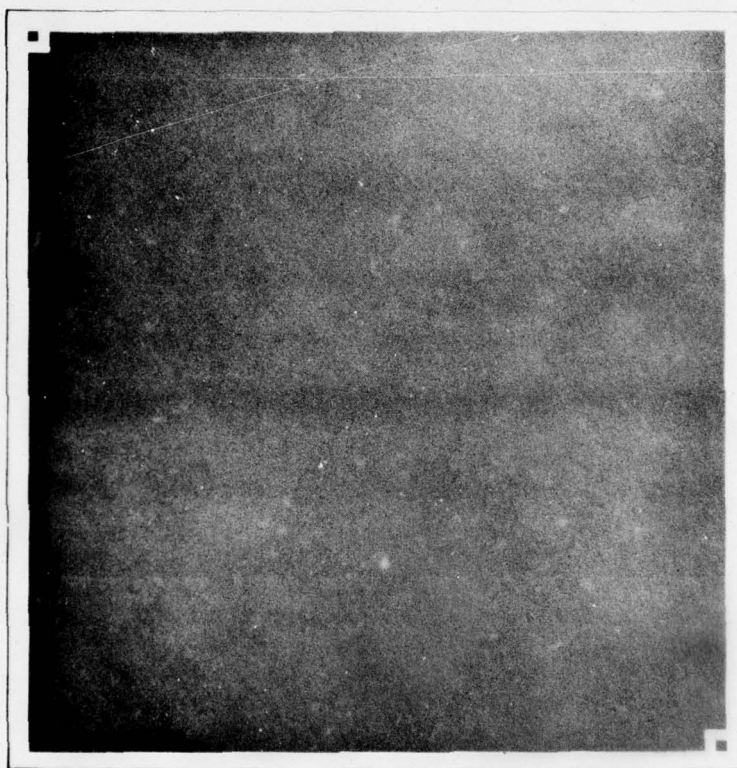
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 8, 2nd metallization layer (voltage plane):



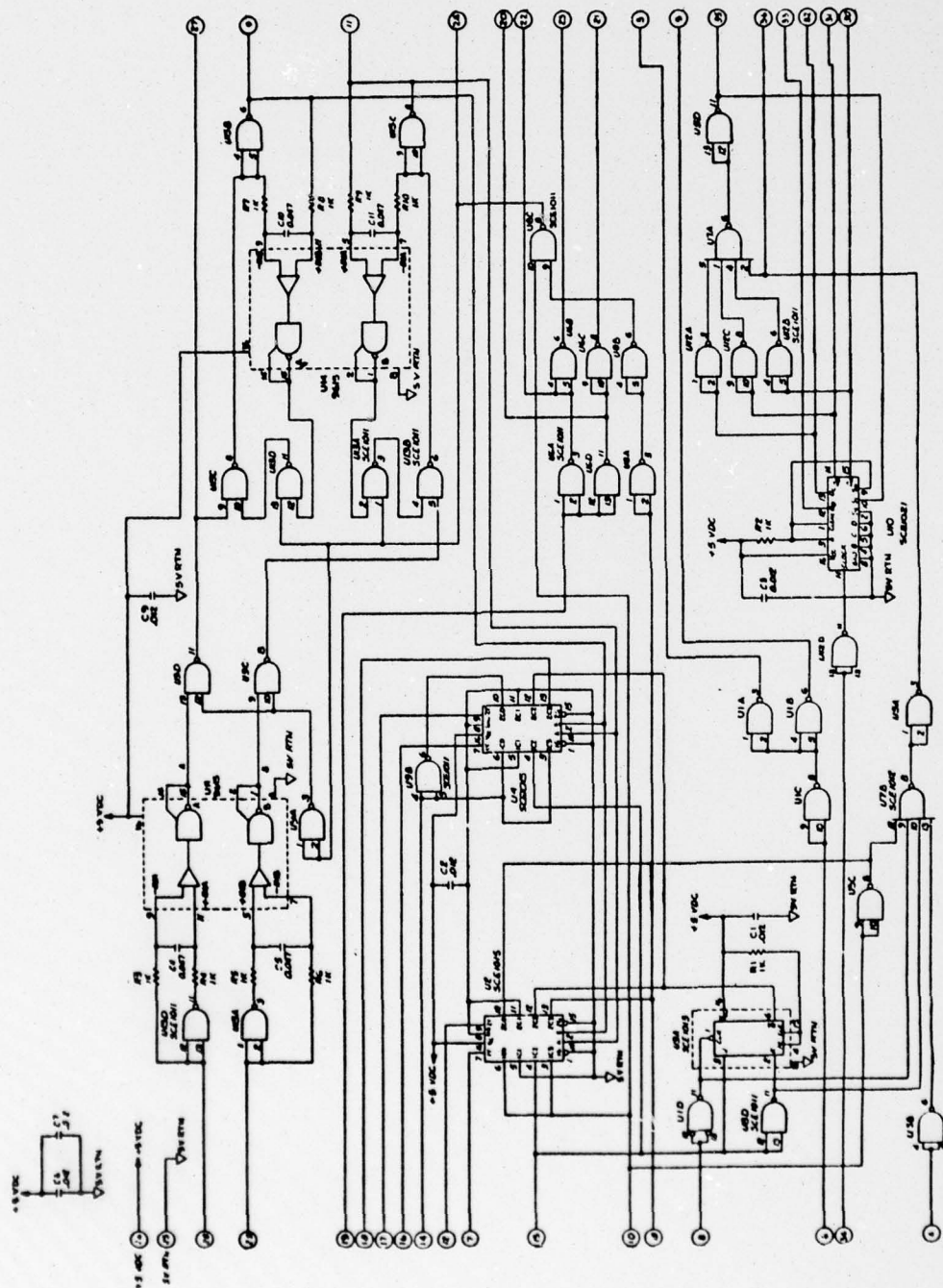
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 8, 1st metallization layer (GND plane):



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9 schematic:



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9 substrate area calculation:

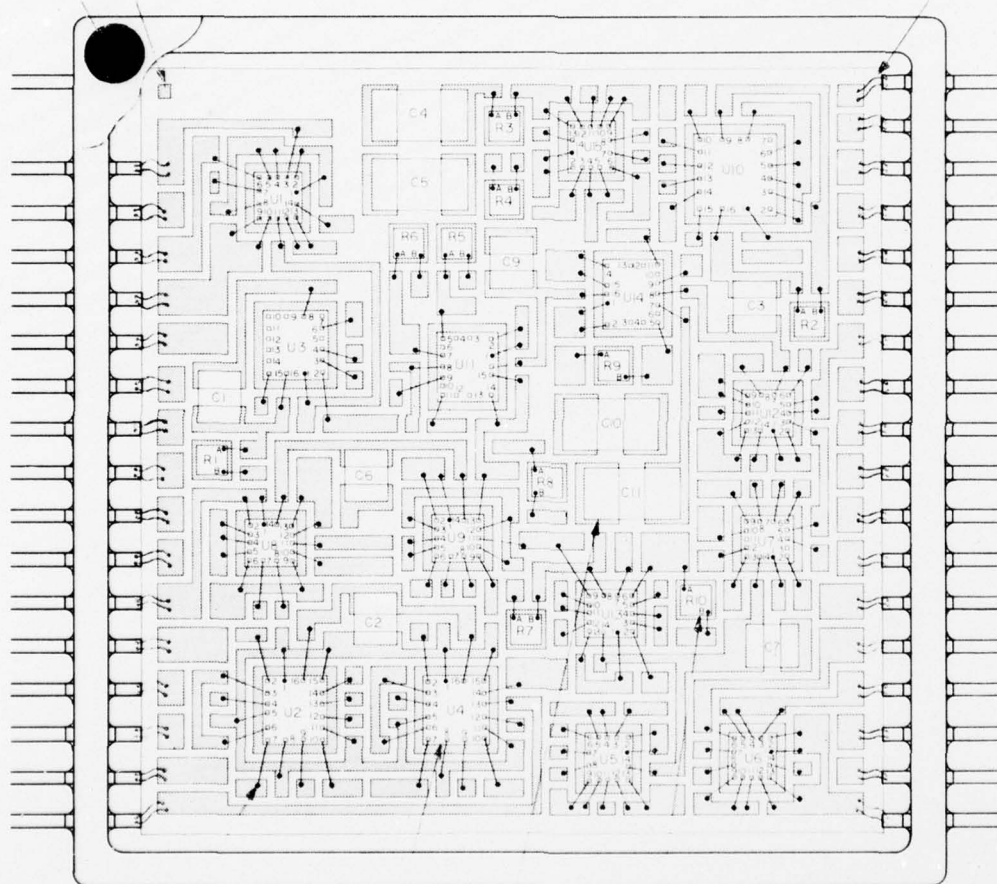
Component Designations	Component Dimensions in. (mm)	Individual Component Area sq in. (sq mm)	Component Area Sub Total		Multiplied Area	
			sq in.	sq mm	sq in.	sq mm
Capacitors: 2x C1, 2, 3, 6, C7, 9	0.050 x 0.060 (1.27 x 1.52)	0.0030 (1.935)	0.0180 (11.613)		0.0360 (23.226)	
C4, 5, 10, 11	0.060 x 0.110 (1.52 x 2.79)	0.0066 (4.258)	0.0264 (17.032)		0.0528 (34.064)	
Resistors: 3x R1 thru 10	0.035 x 0.035 ¹ (0.89 x 0.89)	0.0025 (1.613)	0.0250 (16.129)		0.0750 (48.387)	
I.C.'s: 10x U1, 5, 6, 7, U8, 9, 12, U13, 15	0.055 x 0.060 (1.40 x 1.52)	0.0033 (2.129)	0.0297 (19.161)		0.2970 (191.610)	
U2, 3, 4	0.080 x 0.075 (2.03 x 1.90)	0.0060 (3.871)	0.0180 (11.613)		0.1800 (116.129)	
U10	0.095 x 0.095 (2.41 x 2.41)	0.0090 (5.806)	0.0090 (5.806)		0.0900 (58.060)	
U11, 14	0.080 x 0.070 (2.03 x 1.78)	0.0056 (3.613)	0.0112 (7.226)		0.1120 (72.260)	
			Total =		0.8428 (543.741)	
Actual Substrate Size	0.855 x 0.885 (21.72 x 22.48)	0.7567 (488.192)				

¹ Sizes less than 0.050 x 0.050 in. (1.27 x 1.27 mm) assume 0.050 x 0.050 in. (1.27 x 1.27 mm).

Actual substrate area is 90% of the calculated area.

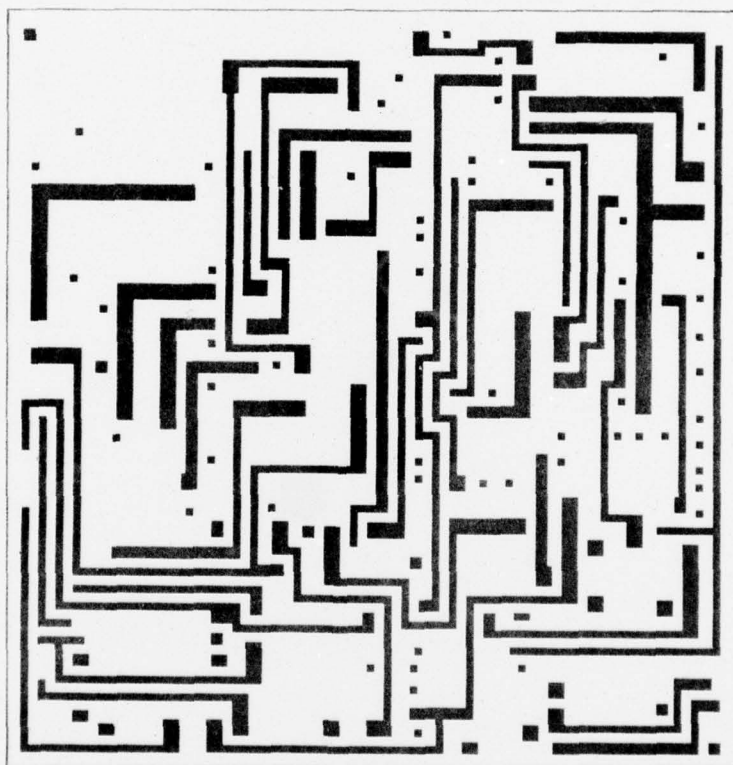
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9 components plus 5th metallization layer:



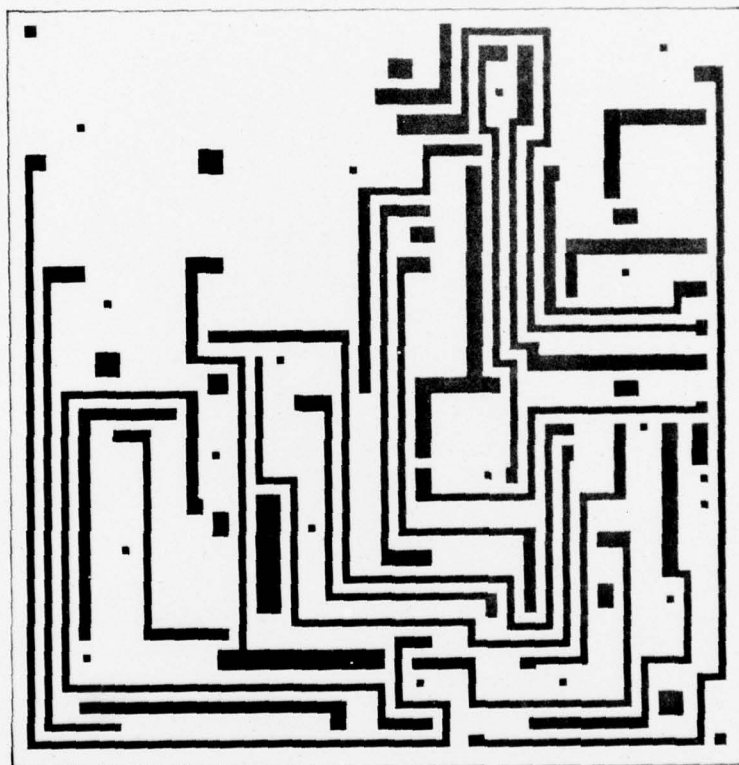
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9, 4th metallization layer (signal interconnections):



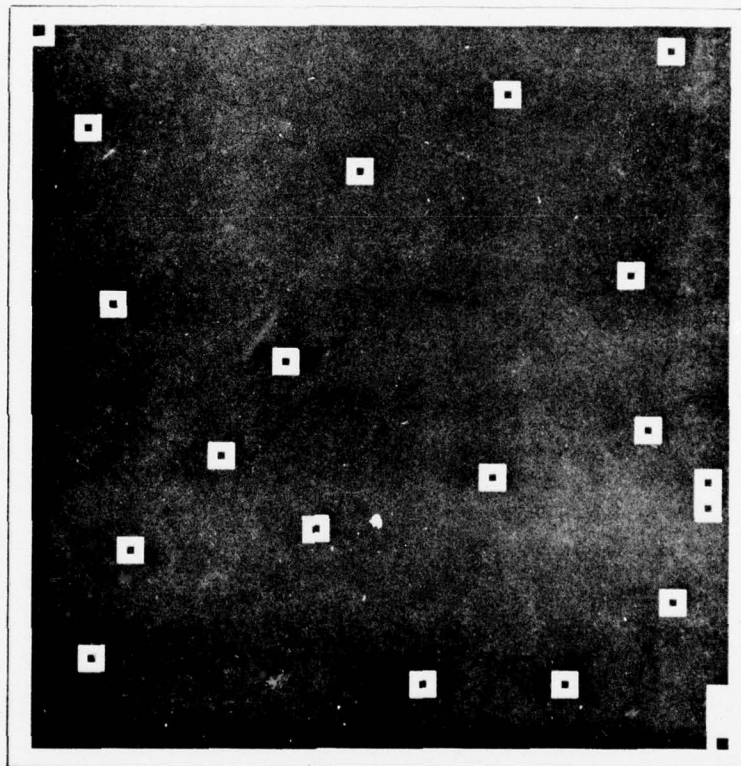
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9, 3rd metallization layer (signal interconnections):



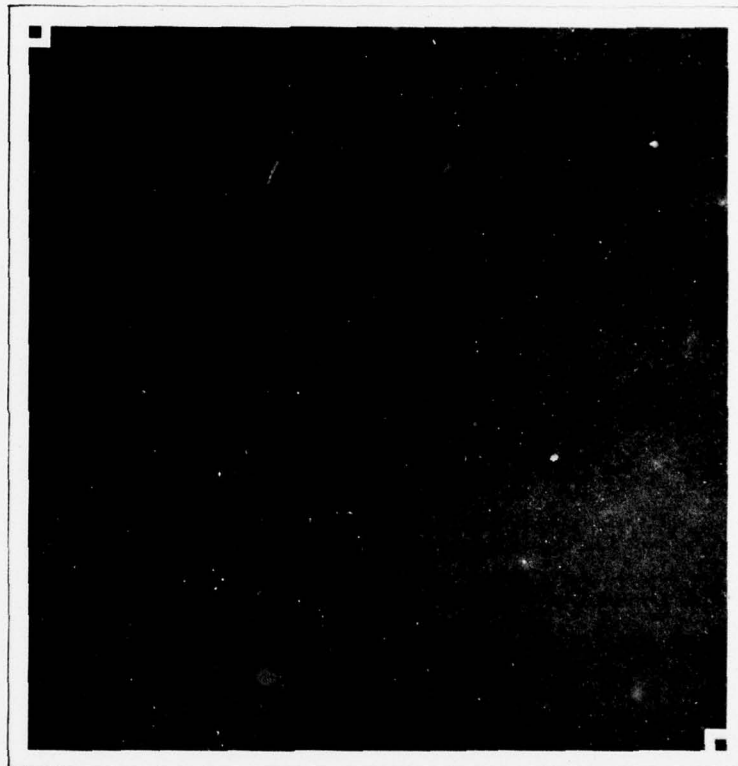
1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9, 2nd metallization layer (voltage plane):



1.8 (Cont.) PACKAGING DENSITY

Circuit No. 9, 1st metallization layer (GND plane):



SECTION 2 ENVIRONMENTAL PARAMETERS (MILITARY STANDARDS)

The information in this section is presented as examples of the environmental stresses that a hybrid must withstand in order to meet the military requirements for high reliability.

The specifications most often imposed to assure high reliability for a hybrid are spelled out in MIL-STD-883 and MIL-STD-38510. All of the specific requirements shown in this text are extracted from revision A of MIL-STD-883. These inclusions are not intended to necessarily show the latest revisions, nor the full content of MIL-STD-883, but rather are indicative of the degree of testing typically required.

MIL-STD-883 describes various tests and assigns to each type of test a designation called a "method number". Within each method there may be subdivisions that specify various degrees of stringencies. These subdivisions are referred to as "Condition" A, B, C, etc.

The list of tests shown in Table 2-1 (as well as each individual method shown in this text) is extracted from the November 15, 1974 issue of MIL-STD-883. It is included here to indicate the categories of tests shown in MIL-STD-883. (Additions and deletions to the specification are made as new techniques and requirements are defined. Obtaining the most up-to-date information requires consulting the latest issue in effect, along with outstanding addenda.) It should be recognized that the specification includes requirements for microelectronic devices other than hybrids, and that not all the tests are applicable to hybrids.

SECTION 2 (Cont.)

ENVIRONMENTAL PARAMETERS
(MILITARY STANDARDS)

Table 2-1 LIST OF METHODS FROM MIL-STD-883

MIL-STD-883A
15 November 1974

TEST METHODS

Method No.

Environmental tests

1001	Barometric pressure, reduced (altitude operation)
1002	Immersion
1003	Insulation resistance
1004.1	Moisture resistance
1005.1	Steady state life
1006	Intermittent life
1007	Agree life
1008.1	High temperature storage
1009.1	Salt atmosphere (corrosion)
1010.1	Temperature cycling
1011.1	Thermal shock
1012	Thermal characteristics
1013	Dew point
1014.1	Seal
1015.1	Burn-in test

Mechanical tests

2001.1	Constant acceleration
2002.1	Mechanical shock
2003.1	Solderability
2004.1	Lead integrity
2005	Vibration fatigue
2006	Vibration noise
2007	Vibration, variable frequency
2008.1	Visual and mechanical
2009.1	External visual
2010.2	Internal visual (monolithic)
2011.1	Bond strength
2012.1	Radiography
2013	Internal visual
2014	Internal visual and mechanical
2015	Resistance to solvents
2016	Physical dimensions
2017	Internal visual (hybrid)
2018	Scanning electron microscope (SEM) inspection of metallization
2019	Die shear test

SECTION 2 (Cont.) ENVIRONMENTAL PARAMETERS
(MILITARY STANDARDS)

Table 2-1 (Cont.) LIST OF METHODS FROM MIL-STD-883

MIL-STD-883A
15 November 1974

TEST METHODS - Continued

Method No.

Electrical tests (digital)

3001.1	Drive source, dynamic
3002.1	Load conditions
3003.1	Delay measurements
3004.1	Transition time measurements
3005.1	Power supply current
3006.1	High level output voltage
3007.1	Low level output voltage
3008.1	Breakdown voltage, input or output
3009.1	Input current, low level
3010.1	Input current, high level
3011.1	Output short circuit current
3012.1	Terminal capacitance
3013.1	Noise margin measurements for digital micro-electronic devices
3014	Functional testing

Electrical tests (linear)

4001	Input offset voltage and current and bias current
4002	Phase margin and slew rate measurements
4003	Common mode input voltage range
	Common mode rejection ratio
	Supply voltage rejection ratio
4004	Open loop performance
4005	Output performance
4006	Power gain and noise figure
4007	Automatic gain control range

Test procedures

5001	Parameter mean value control
5002	Parameter distribution control
5003	Failure analysis procedure for microcircuits
5001.2	Screening procedures
5005.2	Qualification and quality conformance procedures
5006	Limit testing
5007	Wafer lot acceptance

2.1 TEMPERATURE TESTS

The most common temperature stresses imposed on high-reliability hybrids are high temperature storage, temperature cycling and thermal shock all without electrical power; the burn-in test is performed with power on.

2.1.1 High Temperature Storage

The requirements of Method 1008.1, Condition C are common criteria for high temperature storage tests.

METHOD 1008.1

HIGH-TEMPERATURE STORAGE

MIL-STD-883A

15 November 1974

1. PURPOSE. The purpose of this test is to determine the effect on microelectronic devices of storage at elevated temperatures without electrical stress applied. This method may also be used in a screening sequence or as a preconditioning treatment prior to the conduct of other tests. This test shall not be used to determine device failure rates for other than storage conditions. It may be desirable to make end point and, where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanisms with time and temperature.

2. APPARATUS. The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature and suitable electrical equipment to make the specified end point measurements.

3. PROCEDURE. The device shall be stored at the specified ambient conditions for the specified time. Within the time interval of 24 hours before (0 hours before for test durations less than 250 hours) to 72 hours after the specified duration of the test, the device shall be removed from the specified ambient test condition and allowed to reach standard test conditions. When specified, end-point measurements shall be completed within 96 hours after removal of device from the specified ambient test condition. When specified (or at the manufacturer's discretion, if not specified) intermediate measurements shall be made at intermediate points.

3.1 Test condition. The ambient test temperature shall be indicated by specifying a test condition letter from the following table, unless otherwise specified test condition C and a minimum time duration of 24 hours shall apply.

<u>Test condition</u>	<u>Temperature</u>
A	75°C
B	125°C
C	150°C
D	200°C
E	250°C
F	300°C
G	350°C
H	400°C

2.1.1 (Cont.) High Temperature Storage

MIL-STD-883A
15 November 1974

3.1.1 Temperature-accelerated test. A special "testing only" maximum microcircuit rating applicable to high temperature, short-duration testing shall be specified in the applicable procurement document. The rated temperature value should be chosen from the table of 3.1. (To properly select this rating, it is recommended that an adequate sample of devices be exposed to the intended high temperature for at least the corresponding time duration (see figure 1008-1), to ascertain that any failure mechanisms observed do not differ from those observed at lower temperatures over equivalent longer test durations per figure 1008-1.)

At the supplier's option, the specific time and temperature value may be used in conjunction with the graph of figure 1008-1 to establish other testing conditions equivalent to those specified. Allowable equivalent time-temperature combinations shall be chosen by drawing through the point of figure 1008-1 corresponding to the specified time and temperature a straight line parallel to the given regression line, any time-temperature combination which lies on or above this parallel line, within the time limits indicated in figure 1008-1 may be used.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Test condition letter if other than test condition C (see 3.1).
- (b) Test duration if other than 24 hours (see 3.1).
- (c) End point measurements, if applicable (see 3).
- (d) Intermediate measurements, if applicable (see 3).
- (e) Maximum accelerated test temperature rating (see 3.1.1) if applicable.

2.1.1.1 (Cont.) High Temperature Storage

MIL-STD-883A
15 November 1974

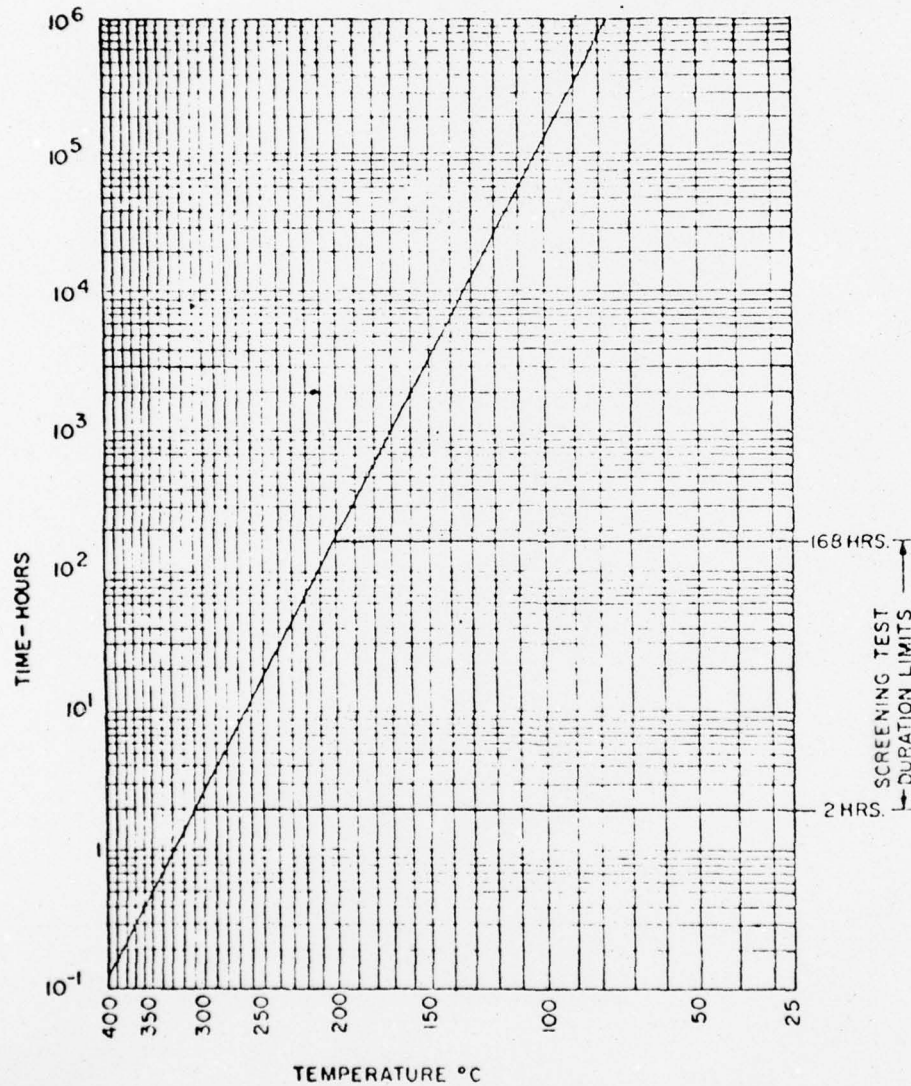


FIGURE 1008-1. Time-temperature regression and allowable time limits for test condition F.

METHOD 1008.1
15 November 1974

2.1.2 Temperature Cycling

The requirements of Method 1010.1, Condition C for 10 cycles are common criteria for temperature cycling.

METHOD 1010.1

MIL-STD-883A
15 November 1974

TEMPERATURE CYCLING

1. **PURPOSE.** This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. These conditions may also be encountered in equipment operated noncontinuous in low-temperature areas or during transportations. Permanent changes in operating characteristics and physical damage produced during temperature cycling result principally from variations in dimensions and other physical properties. Effects of temperature cycling include cracking and delamination of finishes, cracking and crazing of embedding and encapsulating compounds, opening of thermal seals and case seams, leakage of filling materials, and changes in electrical characteristics due to mechanical displacement or rupture of conductors or of insulating materials.

2. **APPARATUS.** Suitable chamber(s) shall be used for the extreme temperature conditions of steps 1 and 3. The air temperature of the chamber(s) shall be held at each of the extreme temperatures by means of circulation and sufficient hot- or cold-chamber thermal capacity so that the ambient temperature measured downstream of the device under test, shall reach the specified temperature within 5 minutes after the specimens have been transferred to the appropriate chamber.

3. **PROCEDURE.** Specimens shall be placed in such a position with respect to the airstream that there is substantially no obstruction to the flow of air across and around the specimen. When special mounting is required, it shall be specified. The specimen shall then be subjected to the specified condition for the specified number of cycles performed continuously. Unless otherwise specified, using test condition C, this test shall be conducted for a minimum 10 cycles. One cycle consists of steps 1 through 4 of the applicable test condition with the duration of exposure at each temperature as indicated in the table of test conditions. Whether single or multiple chambers are used, the effective total transfer time from the specified low temperature to the specified high temperature, or the reverse, shall not exceed 5 minutes. Direct heat conduction to the specimen should be minimized. In the case of multiple chambers, the transfer time shall be defined as the time between withdrawal from the low temperature chamber and introduction into the high temperature chamber.

3.1 **Measurements.** After completion of the final cycle, an external visual examination shall be performed for evidence of defects or damage to case, leads, or seals, or loss of marking legibility, resulting from testing. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence or subgroup of tests which include this test.

2.1.2 (Cont.) Temperature Cycling

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Temperature-cycling test conditions

Step	Minutes	Test condition					
		A Temperature	B Temperature	C Temperature	D Temperature	E Temperature	G Temperature
		°C	°C	°C	°C	°C	°C
1	10 min	-55 +0 -5	-55 +0 -5	-65 +0 -5	-65 +0 -5	-65 +0 -5	-65 +0 -5
2	5 max	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5
3	10 min	85 +3 -0	125 +3 -0	150 +5 -0	200 +5 -0	300 +5 -0	175 +5 -0
4	5 max	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5	25 +10 -5

NOTE: The time at the high and low temperatures shall be sufficient to allow the total mass of each device under test to reach the specified temperature. If carriers or holders employed or other factors make 10 minutes inadequate to allow the mass of each device under test to reach the specified temperature, the time at the temperature extremes shall be increased to meet this requirement. Temperature of worst case loads shall be established with a calibrated thermocouple(s) or other suitable temperature measuring device(s) appropriately placed within the chamber load area.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Special mounting, if applicable (see 3).
- (b) Test condition letter if other than test condition C (see 3).
- (c) Number of test cycles, if other than 10 cycles (see 3).
- (d) End point measurements and examinations (see 3.1) (e.g., end point electrical measurements, seal test (Method 1014) or other acceptance criteria).

METHOD 1010.1
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DESIGN GUIDELINES FOR HYBRID MICROCIRCUITS. VOLUME II. ENGINEER--ETC(U)
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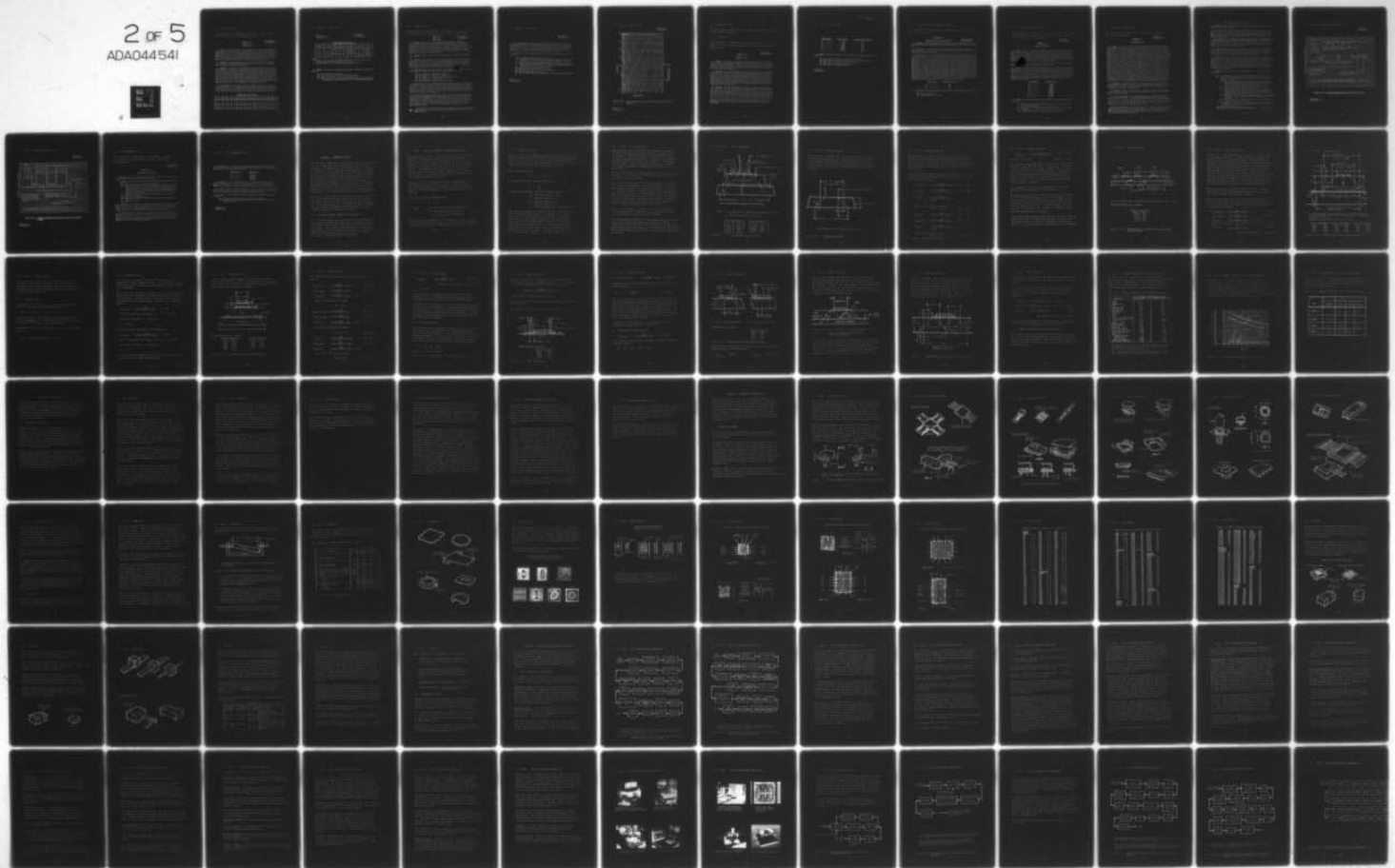
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2.1.3 Thermal Shock

The requirements of Method 1011.1, Condition A for 15 cycles are commonly specified for thermal shock tests.

METHOD 1011.1

MIL-STD-883A
15 November 1974

THERMAL SHOCK

1. **PURPOSE.** The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. These conditions may be encountered in equipment operated intermittently in low temperature areas. Permanent changes in operating characteristics and physical damage produced during temperature shock result principally from variations in dimensions and other physical properties. Effects of thermal shock include cracking and delamination of substrates or wafers, opening of terminal seals and case seams, and changes in electrical characteristics due to moisture effects or to mechanical displacement of conductors or insulating materials.

2. **APPARATUS.** Suitable temperature controlled baths containing liquids shall be chosen to obtain the temperature excursion specified in the table of test conditions (see 3) and within the indicated tolerances.

3. **PROCEDURE.** The device shall be preconditioned by being immersed and in intimate contact with a suitable liquid at the temperature specified in step 1 of the specified test condition for a minimum of 5 minutes. Immediately upon conclusion of the preconditioning time, the device shall be transferred to a liquid at the temperature specified in step 2 of the specified test condition. The device shall remain at the low temperature for a minimum of 5 minutes and then be transferred to a liquid at the step 1 temperature. The device shall remain at the high temperature for a minimum of 5 minutes. Transfer time from high temperature to low temperature and from low temperature to high temperature shall be less than 10 seconds. Unless otherwise specified, using test condition A, the duration of the test shall be 15 complete cycles, where one cycle consists of proceeding from step 1 to step 2 and back to the beginning of step 1.

3.1 **Measurements.** After completion of the final cycle, an external visual examination shall be performed for evidence of defects or damage to case, leads, or seals, or loss of marking legibility resulting from testing. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence or subgroup of test which include this test.

Thermal shock test conditions

Test condition	A	B	C	D	E	F
	Temperature °C	Temperature °C	Temperature °C	Temperature °C	Temperature °C	Temperature °C
Step 1	100 +5 -0	125 +5 -0	150 +5 -0	200 +5 -0	150 +5 -0	200 +5 -0
Step 2	-0 +0 -5	-55 +0 -5	-65 +0 -5	-65 +0 -5	-195 +5 -5	-195 +5 -5

2.1.3 (Cont.) Thermal Shock

METHOD 1011.1
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15 November 1974

Suggested thermal shock fluids

Test condition	A	B	C	D	E	F
	Fluid	Fluids	Fluids	Fluids	Fluids	Fluids
Step 1	Water ^{1/}	FC 70 CR FC40	FC 70 CR FC40	FC 70 CR Silicon oil or UCON 100	FC 70 CR FC40	FC 70 CR Silicon oil or UCON 100
Step 2	Water ^{1/}	FC77	FC77	FC77	Liquid nitrogen	Liquid nitrogen

NOTES:

- ^{1/} Water is indicated as an acceptable fluid for this temperature range; its suitability chemically shall be established prior to use.
2. Ethylene glycol shall not be used as a thermal shock test fluid.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Special mounting, if applicable.
- (b) Test condition if other than test condition A (see 3).
- (c) Number of test cycles if other than 15 cycles (see 3).
- (d) End point measurements and examinations (see 3.1) (e.g., end point electrical measurements, seal test (Method 1014) or other acceptance criteria).

2.1.4 Burn-In Test

The requirements of Method 1015.1, Condition B for 160 hours, minimum, are criteria often specified for the burn-in test.

METHOD 1015.1

MIL-STD-883A
15 November 1974

BURN-IN TEST

1. PURPOSE. The burn-in test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which are evidenced as time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at maximum rated operating conditions or to apply equivalent screening conditions which will reveal time and stress dependent failure modes with equal or greater sensitivity.

2. APPARATUS. Details for the required apparatus shall be as described in Method 1005.

3. PROCEDURE. The microelectronic device shall be subject to the specified burn-in screen test condition (see 3.1) for 160 hours minimum duration and ambient test temperature unless otherwise specified. Lead, stud or case mounted devices shall be mounted by the leads, stud or case in their normal mounting configuration and the point of connection shall be maintained at a temperature not less than the specified temperature. Pre and post burn-in measurements shall be made as specified.

3.1 Test conditions. Basic test conditions are as shown below. Details for each of these conditions, except where noted, shall be as described in Method 1005.

- (a) Test condition A: Steady-state, reverse bias.
- (b) Test condition B: Steady-state, power.
- (c) Test condition C: Steady-state, power and reverse bias.
- (d) Test condition D: Parallel, series excitation.
- (e) Test condition E: Ring oscillator.
- (f) Test condition F: Temperature-accelerated power.

3.2 Measurements. Pre burn-in measurements, when specified, shall be conducted prior to applying burn-in test conditions. Unless otherwise specified, post burn-in measurements shall be completed within 96 hours after removal of the devices from the specified burn-in test condition and shall include all 25°C DC parameter measurements (subgroup A-1 of method 5005) and all parameters for which delta limits have been specified as interim (post burn-in) electrical measurements. Delta limit acceptance when applicable shall be based on this measurement within 96 hours.

3.2.1 Measurements following reverse bias life. When devices are measured following application of test condition A, C or F, they shall be cooled to room temperature prior to the removal of bias. Alternatively, unless otherwise specified, the bias may be removed during cooling provided the case temperature of devices under test is reduced to a maximum of 35°C within 30 minutes after removal of the test conditions. All specified 25°C electrical measurements shall be completed prior to any reheating of the devices and all specified electrical measurements shall be completed within 96 hours after removal of life test bias.

* "Interruption of bias(es) during transfer of devices between bias supplies for cooldown (total time of interruption less than one minute) shall not be considered removal of bias."

2.1.4 (Cont.) Burn-In Test

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3.2.2 Test monitoring. The test setup shall be monitored at least initially and at the conclusion of the test to establish that all devices are being stressed as required for the specific test condition. Each device does not have to be checked but sampling techniques may be used. Where failures occur which result in removal of the required test stresses for any period of the required duration (see 3.1), the test shall be continued to assure actual exposure for the total minimum specified duration.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Test duration if other than 160 hours (see 3).
- (b) Test condition letter and burn-in test circuit with appropriate details for inputs, outputs, biases, and power dissipation as applicable (see 3.1).
- (c) Burn-in test temperature and whether ambient or case (see 3). Unless otherwise specified, the test temperature shall be the maximum ambient operating temperature of the device being tested.
- (d) Test mounting, if other than normal (see 3).
- (e) Pre burn-in measurements when applicable (see 3.2).
- (f) Special maximum test rating for test condition F.
- (g) Post burn-in measurements (see 3.2).
- (h) Time to complete post burn-in measurements if other than specified (see 3.2).

METHOD 1015.1
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2.1.4 (Cont.) Burn-In Test

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15 November 1974

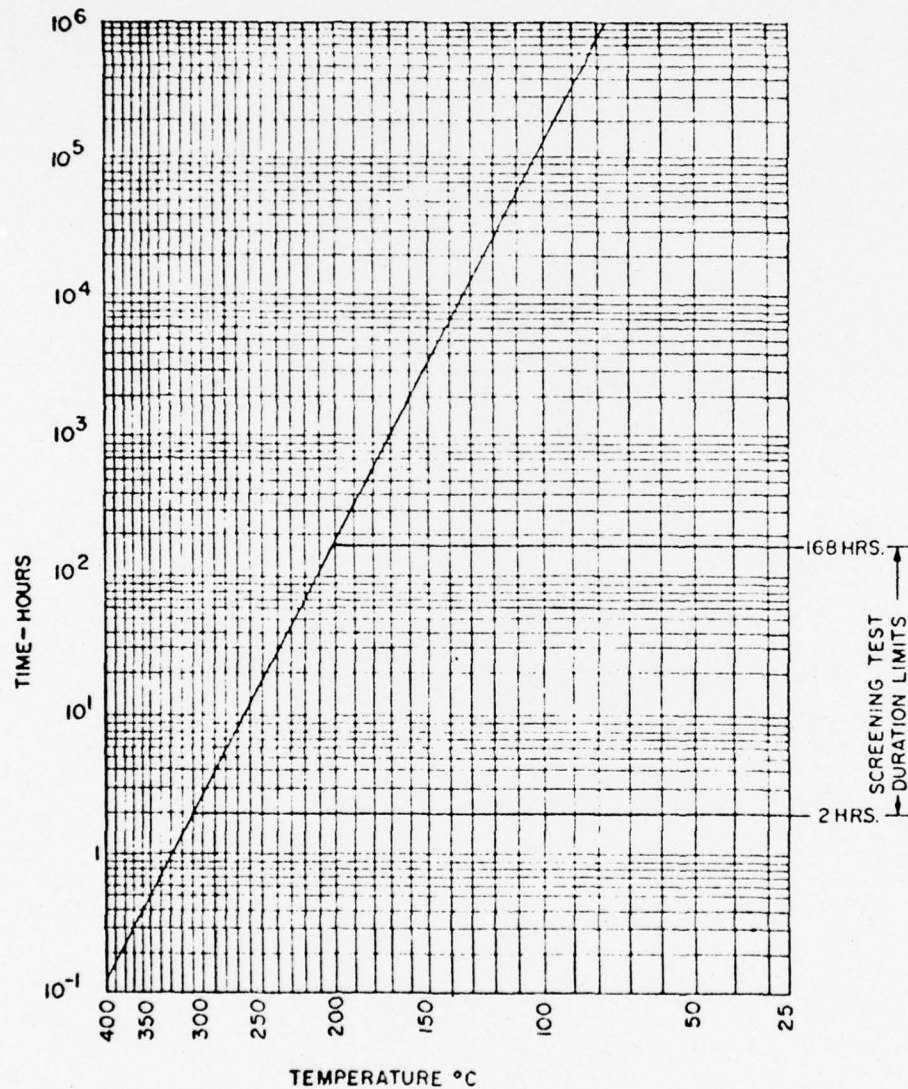


FIGURE 1015-1. Time-temperature regression and allowable time limits for test condition F.

METHOD 1015.1
15 November 1974

2.2 MECHANICAL TESTS

The most common mechanical stresses required are shock, vibration, and constant acceleration.

2.2.1 Shock Test

The requirements of Method 2002.1, Condition B, for five (5) shocks in six (6) directions are often specified for mechanical shock testing.

MIL-STD-883A
15 November 1974

METHOD 2002.1

MECHANICAL SHOCK

1. **PURPOSE.** The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

2. **APPARATUS.** The shock-testing apparatus shall be capable of providing shock pulses of 500 to 30,000 G (peak) as specified with a pulse duration between 0.1 and 1.0 msec, to the body of the device. The acceleration pulse, as determined from the unfiltered output of a transducer with a natural frequency greater than or equal to five times the frequency of the shock pulse being established, shall be a half-sine waveform with an allowable distortion not greater than ± 20 percent of the specified peak acceleration. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ± 0.1 millisecond or ± 30 percent of the specified duration.

3. **PROCEDURE.** The shock-testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Means may be provided to prevent the shock from being repeated due to "bounce" in the apparatus. Unless otherwise specified, the device shall be subject to 5 shock pulses of the peak (G) level specified in the selected test condition and for the pulse duration specified in each of the orientations X_1 , X_2 , Y_2 , Y_1 , Z_1 , and Z_2 . For devices with internal elements mounted with the major plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount (orientations of 4.4 of the general requirements notwithstanding). Unless otherwise specified, test condition B shall apply.

2.2.1 (Cont.) Shock Test

<u>Test condition</u>	<u>G Level (peak)</u>	<u>Duration of pulse (msec)</u>
A - - - - -	500	1.0
B - - - - -	1,500	0.5
C - - - - -	3,000	0.3
D - - - - -	5,000	0.3
E - - - - -	10,000	0.2
F - - - - -	20,000	0.2
G - - - - -	30,000	0.12

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Test condition if other than test condition B (see 3).
- (b) Number and direction of shock pulses if other than specified (see 3).
- (c) Electrical-load conditions, if applicable (see 3).
- (d) When required, measurement made after test.
- (e) When required, measurement during test.

METHOD 2002.1
15 November 1974

2.2.2 Vibration Test (Variable Frequency)

The requirements of Method 2007, Condition A are common criteria for vibration tests.

METHOD 2007

VIBRATION, VARIABLE FREQUENCY

MIL-STD-883A
15 November 1974

1. **PURPOSE.** The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range. This is a destructive test.
2. **APPARATUS.** Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels and the necessary optical and electrical equipment for post-test measurements.
3. **PROCEDURE.** The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. Lead-mounted devices shall be mounted by their leads in the normal mounting configuration. The device shall be vibrated with simple harmonic motion having an amplitude of either 0.06 inches double amplitude (maximum total excursion) or the peak acceleration for test condition A, B, or C, as specified, whichever is less. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range of 20 to 2,000 Hz and return to Hz shall be traversed in not less than 4 minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (total of 12 times), so that the motion shall be applied for a total period of approximately 48 minutes, minimum. Following vibration, the device shall be subjected to the specified post-test measurements and to an external visual examination at a magnification between 10X and 20X for evidence of damage to package, leads, seals, and markings. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

<u>Test condition</u>	<u>Peak acceleration, G</u>
A - - - - -	20
B - - - - -	50
C - - - - -	70

4. **SUMMARY.** The following details shall be specified in the applicable procurement document:
 - (a) Test condition (see 3).
 - (b) Measurements after test (see 3).

2.2.3 Constant Acceleration

The requirements of Method 2001.1, in the Y_1 direction is common. For large hybrids, Condition A is often specified; for small hybrids Condition D is more common.

MIL-STD-883A
15 November 1974

METHOD 2001.1

CONSTANT ACCELERATION

1. **PURPOSE.** This test is used to determine the effects of constant acceleration on microelectronic devices. It is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. It may be used as a high stress test to determine the mechanical limits of the package, internal metallization and lead system, die or substrate attachment, and other elements of the microelectronic device. By establishing proper stress levels, it may also be employed as an in-line 100 percent screen to detect and eliminate devices with lower than nominal mechanical strengths in any of the structural elements.

2. **TEST EQUIPMENT.** Constant acceleration tests shall be made on an apparatus capable of applying the specified acceleration for the required time.

3. **PROCEDURE.** The device shall be restrained by its case, or by normal mountings, and the leads or cables secured. Unless otherwise specified, a constant acceleration of the value specified shall then be applied to the device for 1 minute in each of the orientations X_1 , X_2 , Y_2 , Y_1 , Z_1 , and Z_2 . For devices with internal elements mounted with the major seating plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount (orientations of paragraph 4.4 of general requirements notwithstanding). Unless otherwise specified, test condition E shall apply.

<u>Test condition</u>	<u>Stress level (g)</u>
A - - - - -	5,000
B - - - - -	10,000
C - - - - -	15,000
D - - - - -	20,000
E - - - - -	30,000
F - - - - -	50,000
G - - - - -	75,000
H - - - - -	100,000
J - - - - -	125,000

4. **SUMMARY.** The following details shall be specified in the applicable procurement document:

- (a) Amount of acceleration to be applied, in gravity units (g) if other than test condition E (see 3).
- (b) When required, measurements to be made after test.
- (c) Any variations in duration or limitations to orientation (e.g., Y_1 only) (see 3).
- (d) Sequence of orientations if other than as specified (see 3).

2.3 MOISTURE RESISTANCE TEST

The requirements of Method 1004.1 are commonly invoked for moisture resistance tests.

MIL-STD-883A
15 November 1974

METHOD 1004.1

MOISTURE RESISTANCE

1. **PURPOSE.** The moisture resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of component parts and constituent materials to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals; physical distortion and decomposition of organic materials; leaching and consuming constituents of materials; and detrimental changes in electrical properties. This test differs from the steady-state humidity test and derives its added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes and, in addition, produces a "breathing" action of moisture into partially sealed containers. Increased effectiveness is also obtained by use of a higher temperature, which intensifies the effects of humidity. The test includes a low-temperature subcycle that acts as an accelerant to reveal otherwise undiscernible evidences of deterioration since stresses caused by freezing moisture tend to widen cracks and fissures. As a result the deterioration can be detected by the measurement of electrical characteristics (including such tests as voltage breakdown and insulation resistance) or by performance of a test for sealing. Provision is made for the application of a polarizing voltage across insulation to investigate the possibility of electrolysis, which can promote eventual dielectric breakdown. This test also provides for electrical loading of certain components, if desired, in order to determine the resistance of current-carrying components, especially fine wires and contacts, to electro-chemical corrosion. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. This test has proved reliable for indicating those parts which are unsuited for tropical field use.

2. **APPARATUS.** The apparatus used for the moisture resistance test shall include temperature-humidity chambers capable of maintaining the cycles and tolerances described in figures 1004-1 or 1004-2 and electrical test equipment capable of performing the measurements in paragraph 3.6 and paragraph 4.

3. **PROCEDURE.** Specimens shall be tested in accordance with 3.1 thru 3.6 inclusive, and figures 1004-1 or 1004-2. Specimens shall be mounted in a manner that will expose them to the test environment.

3.1 **Initial conditioning.** Prior to mounting specimens for the moisture resistance test, the device leads shall be subjected to a bending stress, initial conditioning in accordance with test condition B₁ of Method 2004, unless otherwise specified. Where the specific sample devices being subjected to the moisture resistance test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

3.2 **Initial measurements.** Prior to step 1 of the first cycle, the specified initial measurements shall be made at room ambient conditions, or as specified. When specified, the initial conditioning in a dry oven (see figure 1004-1 or 1004-2 as applicable) shall precede initial measurements and the initial measurements shall be completed within 8 hours after removal from the drying oven.

2.3 (Cont.) MOISTURE RESISTANCE TEST

3.3 Number of cycles. Specimens shall be subjected to 10 continuous cycles, each as shown on figure 1004-1 or 1004-2.

3.4 Subcycle. During step 7, at least 1 hour but not more than 4 hours after step 7 begins, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced, for performance of step 7a. After step 7a, the specimens shall be returned to 25°C at 90 to 98 percent relative humidity (RH) and kept there until the next cycle begins. This subcycle shall be performed during any five of the first nine cycles.

3.4.1 Step 7a. At least 1 hour but not more than 4 hours after the beginning of step 7, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced. Specimens shall then be conditioned at $-10^{\circ} \pm 2^{\circ}\text{C}$, with humidity not controlled, for 3 hours as indicated on figure 1004-1 or 1004-2. When a separate cold chamber is not used, care should be taken to assure that the specimens are held at $-10^{\circ} \pm 2^{\circ}\text{C}$, for the full 3-hour period.

3.5 Applied voltage. During the moisture resistance test as specified in figure 1004-1 or 1004-2, when specified (see 4), the device shall be biased in accordance with the specified bias configuration which should be chosen to maximize the voltage differential between chip metallization runs or external terminals, minimize power dissipation and to utilize as many terminals as possible to enhance test results.

3.6 Final measurements. Following step 6 of the final cycle, devices shall be conditioned for 24 hours at room ambient conditions after which an insulation resistance test shall be performed in accordance with Method 1003, test condition A. The insulation resistance test must be completed within 48 hours after removing the devices from the chamber. The measured resistance shall be no less than 10 megohms. When the insulation resistance test is performed, it must be recorded and data submitted as part of the Group C end point data. The insulation resistance test may be omitted provided the specified 25°C electrical end point measurements are completed within 48 hours after removal of the device from the chamber.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Initial measurements, and conditions if other than room ambient (see 3.2).
- (b) Applied voltage, when applicable (see 3.5) and bias configuration when required. This bias configuration shall be chosen in accordance with the following guidelines:
 - (1) Only one supply voltage (V) either positive or negative is required, and an electrical ground (or common terminal) GND. The magnitude of V will be the maximum such that the specified absolute maximum ratings are not exceeded and test conditions are optimized.
 - (2) All normally specified voltage terminals and ground leads shall be connected to GND unless otherwise specified.
 - (3) All data inputs, unless otherwise specified, shall be connected to V. The polarity and magnitude of V is chosen to minimize internal power dissipation and current flow into the device. All extender inputs shall be connected to GND unless otherwise specified.
 - (4) All additional leads, e.g., clock, set, reset, outputs, etc., considered individually, shall be connected to V or GND whichever minimizes current flow.
 - (5) Leads with no internal connection shall be biased to V or GND whichever is opposite to an adjacent lead.
- (c) Final measurements (see 3.6). Final measurements shall include all electrical characteristics and parameters which are specified as end point electrical parameters.
- (d) Number of cycles if other than 10 (see 3.3).
- (e) Conditioning in dry oven before initial measurements, if required (see 3.2).

2.3 (Cont.) MOISTURE RESISTANCE TEST

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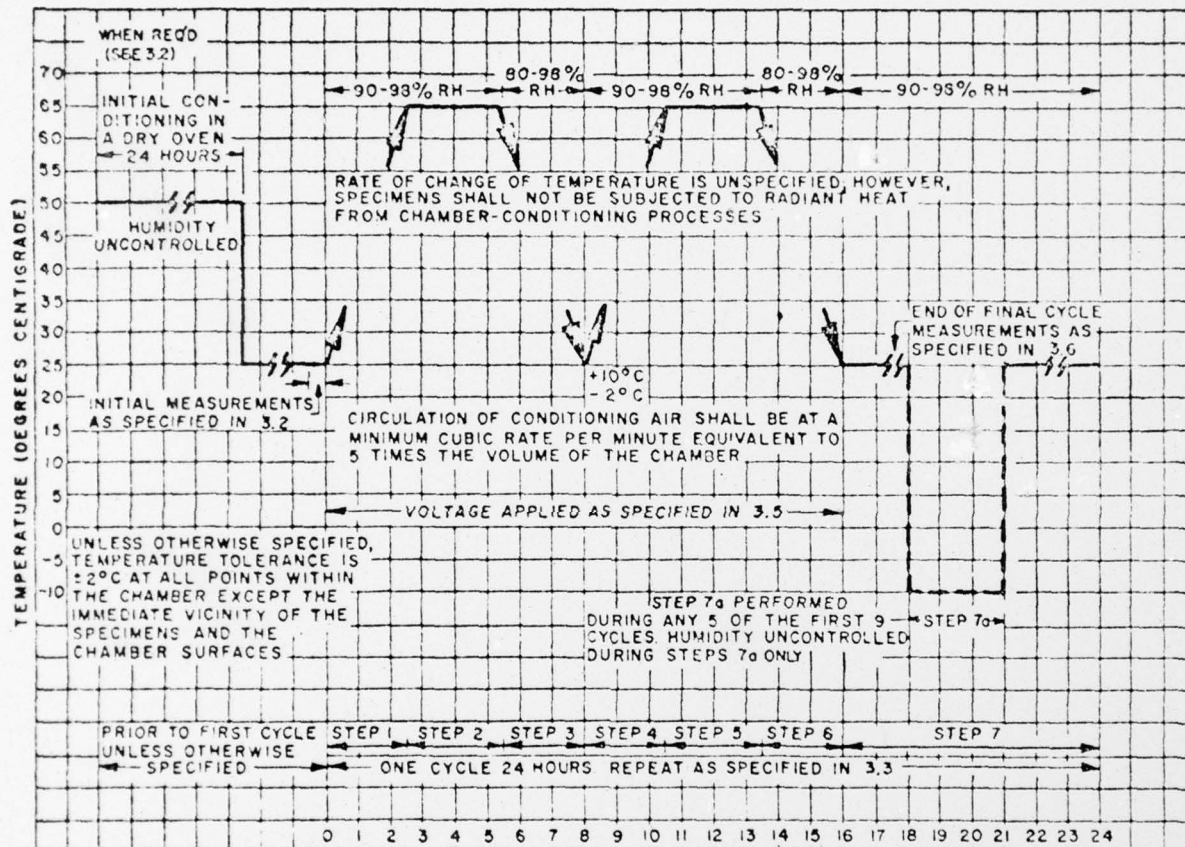


FIGURE 1004-1. Graphical representation of moisture-resistance test.

METHOD 1004.1
15 November 1974

2.3 (Cont.) MOISTURE RESISTANCE TEST

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15 November 1974

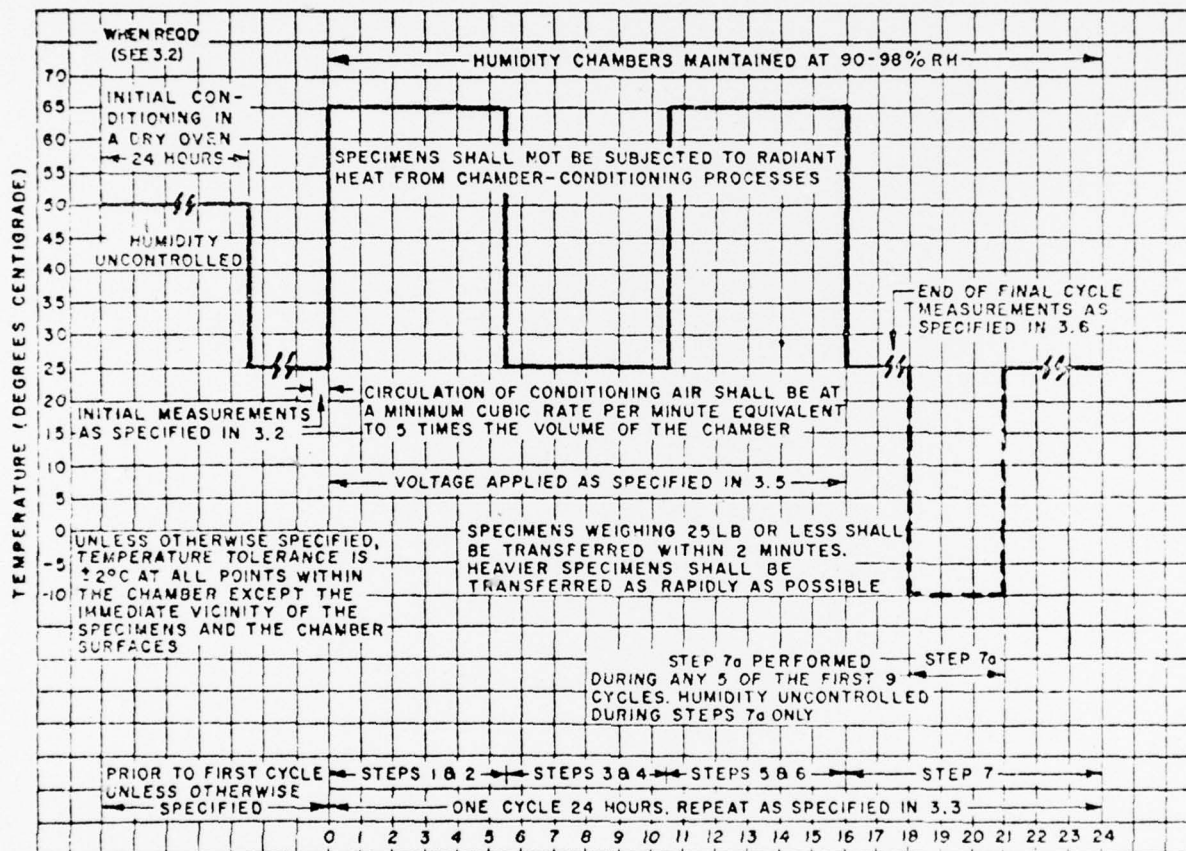


FIGURE 1004-2. Graphical representation of moisture-resistance test (alternate method).

METHOD 1004.1
15 November 1974

2.4 SALT ATMOSPHERE TEST

The requirements of Method 1009.1, Condition A, are common criteria for testing the hybrid's ability to withstand salt atmosphere.

MIL-STD-283A
15 November 1974

METHOD 1009.1

SALT ATMOSPHERE (CORROSION)

1. PURPOSE. This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmospheres on devices.
2. APPARATUS. Apparatus used in the salt-atmosphere test shall include the following:
 - (a) Exposure chamber with racks for supporting devices.
 - (b) Salt-solution reservoir. (The salt used shall be sodium chloride containing on a dry basis not more than 0.1 percent of sodium iodide, and not more than 0.3 percent of total impurities. Distilled or other water used in the preparation of solutions shall contain not more than 200 parts per million of total solids. The solution shall be kept free from solids by filtration or decantation.)
 - (c) Means for atomizing the salt solution, including suitable nozzles and compressed-air supply.
 - (d) Chamber-heating means and controls.
 - (e) Means for humidifying the air at a temperature above the chamber temperature.
 - (f) Magnifier 5X to 10X.
3. PROCEDURE. After initial conditioning in accordance with 3.1, the device shall be placed within the test chamber. A salt atmosphere fog having a temperature of 35°C (95°F) shall be passed through the chamber for the specified test duration (see test conditions below). The fog concentration and velocity shall be so adjusted that the rate of salt deposit in the test area is between 10,000 and 50,000 mgm/m²/day.
 - 3.1 Initial conditioning. Prior to mounting specimens for the salt-atmosphere test, the device leads shall be subjected to a bending stress, initial conditioning in accordance with test condition B₁ of Method 2004, unless otherwise specified. Where the specific sample devices being subjected to the salt atmosphere test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

2.4 (Cont.) SALT ATMOSPHERE TEST

3.2 Length of test. The duration of exposure to the salt-atmosphere test shall be specified by specifying a test condition letter from the following table. Unless otherwise specified, test condition A shall apply.

<u>Test condition</u>	<u>Length of test</u>
A - - - - -	24 hours
B - - - - -	48 hours
C - - - - -	96 hours
D - - - - -	240 hours

3.3 Examination. Upon completion of the test, and to aid in the examinations, devices shall be prepared in the following manner, unless otherwise specified: Salt deposits shall be removed by a gentle wash or dip in running water not warmer than 100°F (37.8°C) and a light brushing, using a soft-hair brush or soft plastic bristle brush.

3.3.1 Failure criteria. A device with illegible markings or when using a magnification of 5X to 10X, evidence of corrosion or flaking or pitting of the finish that will interfere with the application of the device shall be considered a failure.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

- (a) Test condition, if other than test condition A (see 3.2).
- (b) Measurements and examinations after test, when applicable for other than visual (see 3.3).

METHOD 1009.1
15 November 1974

SECTION 3 THERMAL EVALUATION

Most electronic components, especially resistors and semiconductor devices, generate heat in the performance of their electronic functions. The temperature at which they operate is determined by the amount of heat generated by the components, the temperature of the environment, and the heat-transfer characteristics of the materials between the heat sources and the environment. Most components are rated by their manufacturers as to their maximum operating temperatures, above which the component's performance may be degraded or may totally fail. An adequate thermal design insures that the heat generated within each component will flow to the environment so that the operating temperature of the component will not exceed its rated maximum.

The figure of three watts per square inch has often been used as a safe limit for the total dissipation within a package (the square inch units refer to the base area of the package), but this generalization gives no information about individual hot spots within that package. The following text describes thermal evaluations of individual components.

3.1 ELEMENTARY THERMAL COMPUTATION TECHNIQUES

This section describes thermal characteristics and procedures for determining approximate temperature differences between the package surface and the heat generating elements within the package. This elementary presentation will not discuss the complexities of determining the difference in temperature between the ambient air and the package surface. Such a discussion is beyond the intent of this text.

3.1 (Cont.) ELEMENTARY THERMAL COMPUTATION TECHNIQUES

Throughout this section, it will be assumed that the conditions being analyzed are steady-state, rather than fluctuating conditions. Of the three possible modes of heat transfer (conduction, convection, radiation) conduction is the one primarily applicable to hybrids, and is the only one discussed in this section. Any additional heat transfer due to convection or radiation can be considered a bonus. However, since the amount of that bonus is not measured, the thermal design should insure that conduction alone is sufficient.

The basic concept is that the difference in temperature (i.e., temperature rise) between the case surface and the heat producing element depends upon the thermal resistance in the heat flow path and upon the amount of power being dissipated in the element.

This concept expressed mathematically:

$$\Delta T = RP \quad (1)$$

where ΔT is the difference in temperature, $^{\circ}\text{C}$
 R is the thermal resistance, $^{\circ}\text{C}/\text{W}$
 P is the power being dissipated, W

The difference in temperature can be expressed as $(T_1 - T_2)$, where T_1 is the temperature of the heat source and T_2 is the temperature of the outer case surface. Substituting into Equation (1) gives:

$$(T_1 - T_2) = RP \quad (2)$$

3.1.1 Thermal Resistance

Thermal resistance, as applied to hybrid microcircuits, typically means the thermal resistance between the power dissipating element and the outer surface of the package case. When the heat flow path is through several different materials in a series, the total resistance is the sum of the individual resistances.

Expressed mathematically:

$$R = R_1 + R_2 + R_3 \quad (3)$$

The thermal resistance through one material is:

$$R_1 = \frac{X}{K_1 A_1} \quad (4)$$

in which the common mixed (metric and English) units are:

R_1 = thermal resistance, $^{\circ}\text{C}/\text{W}$

X = material thickness, in.

K_1 = thermal conductivity of material, $\text{W}/^{\circ}\text{C (in.)}$

A_1 = cross-sectional area of heat path, in.^2

This expression (Equation 4) defines only the predictable resistance through the material itself. An additional resistance exists at the interface between two materials. The amount of interface resistance depends primarily on the total surface contact between the bonding agent and the two materials. Air gaps between the surfaces increase the interface resistance. Solder bonds and eutectic bonds create good molecular interfaces with very low resistances (assuming no gaps within the total bonded areas). Epoxies, on the other hand, do not create

3.1.1 (Cont.) Thermal Resistance

molecular bonds and can also have high interface resistances arising from tiny gaps caused by the surface roughness of the two materials. Empirical testing of epoxy bonds has demonstrated an increase in resistance of as much as 20% above that predicted for the epoxy itself, and as much as a 10% increase in solder bonds. Later calculations in this text will arbitrarily add 5% resistance to each solder joint and 10% to each epoxy joint.

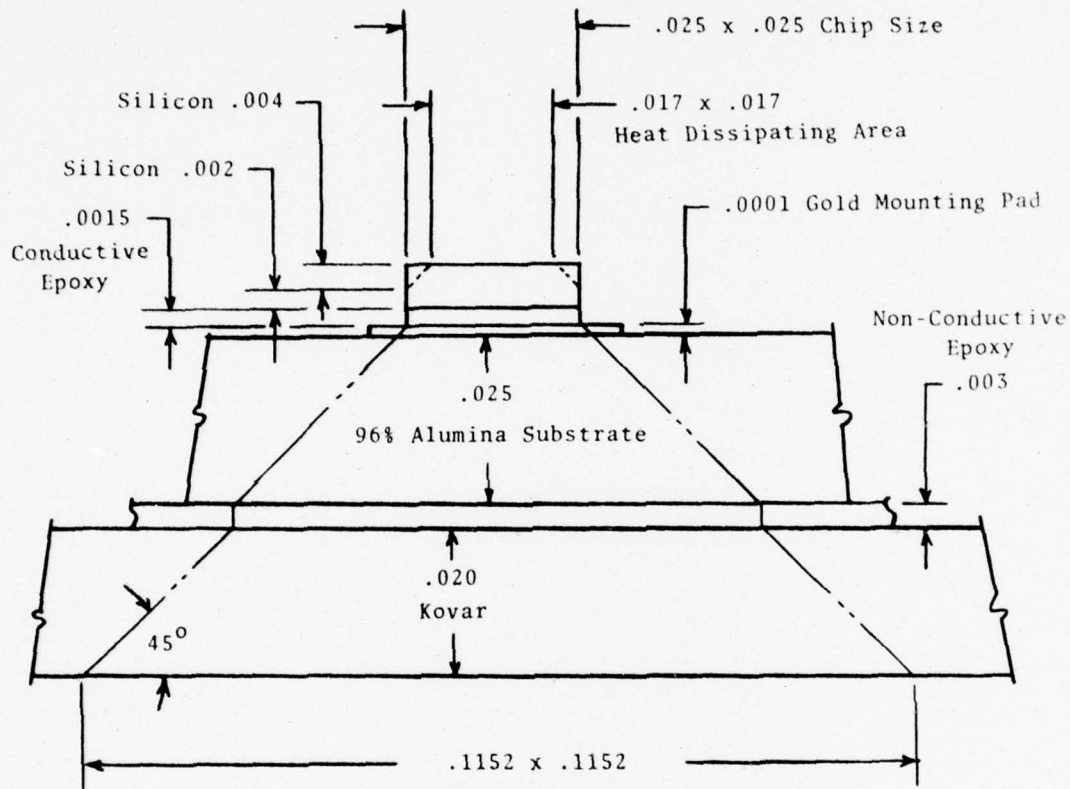
Thermal conductivity is an inherent property of the material being considered. In Section 3.3, the thermal conductivity is given for various hybrid materials.

The cross-sectional area of the heat path should be calculated one of two ways, depending on the configuration of the material. One calculation method is used when the heat-path cross section is a vertical column with a constant cross section throughout the thickness involved. The other method assumes that the heat path is spreading out at a 45 degree angle because the material through which the heat will flow is wider than the dissipating element. Both methods are usually required when computing the total resistance through several types of materials.

Figure 3.1.1-1 depicts a sectional view of a typical hybrid. A semiconductor chip is mounted on a ceramic substrate, which is in turn mounted within a kovar-metal package.

The heat-generating elements of a semiconductor chip are located inside the chip near the top surface, and do not usually occupy the entire surface area. For the purposes of simplifying calculations, assume that the heat is dissipated over the central half of the surface area, and that it is dissipated on the surface of the chip.

3.1.1 (Cont.) Thermal Resistance



NOTE: No appreciable spreading thru the epoxy bonds.

- NOTE: 1. No appreciable spreading through the epoxy bonds.
2. Dimensions shown are in inches.

Metric Equivalents

in.	mm
.0001	.0025
.0015	.0381
.0020	.0508
.0030	.0762
.0040	.1016

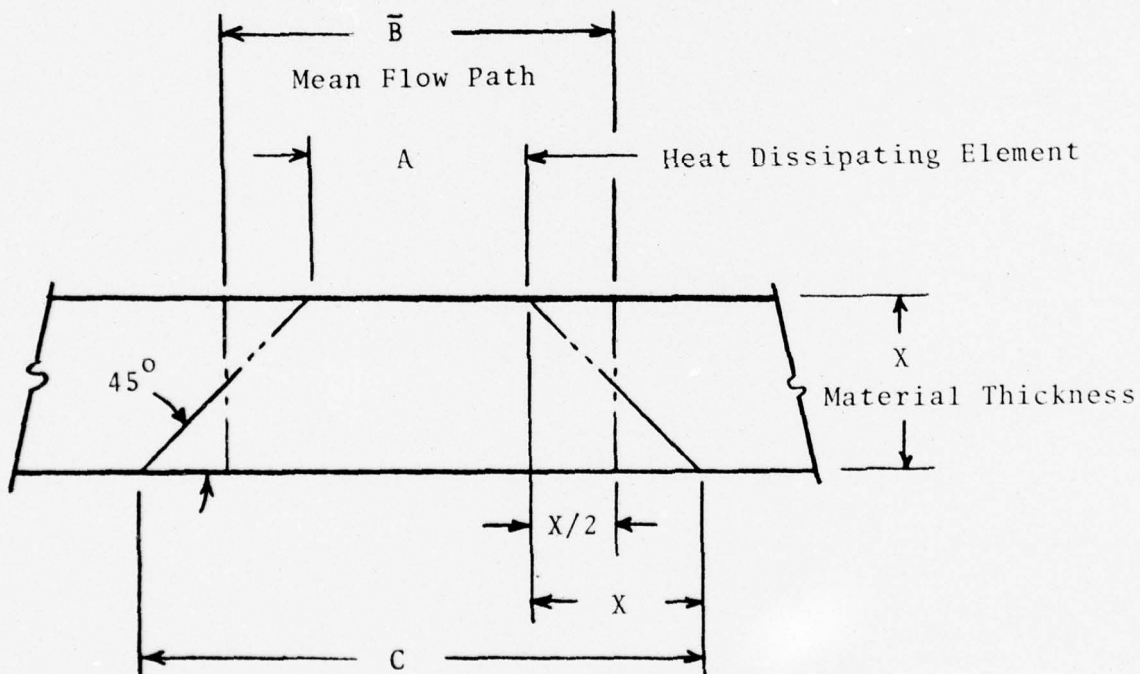
Metric Equivalents

in.	mm
.0170	.4318
.0200	.5080
.0250	.6350
.1152	2.9261

Figure 3.1.1-1 TYPICAL HYBRID HEAT-FLOW PATH

3.1.1 (Cont.) Thermal Resistance

When the heat is spreading, the cross section of the heat path is constantly increasing. This complex shape can be converted to an equivalent simple shape, called the mean-flow path, which is the average cross section between the smallest and the largest cross sections. Figure 3.1.1-2 is an illustration of the mean-flow path.



Mean-flow path \bar{B} is midway between A and C .

Figure 3.1.1-2 MEAN HEAT-FLOW PATH

3.1.1 (Cont.) Thermal Resistance

Referring back to Figure 3.1.1-1, the cross-sectional area through the silicon chip should be calculated in two parts. For the first 4 mils the heat will be spreading, therefore the mean-flow path is applicable. Then, because the heat can not spread any further, the actual chip dimensions dictate the cross section.

Using the values of thermal conductivity from Section 3.3, the thermal resistance of the heat flow path in Figure 3.1.1-1 can be calculated as follows:

$$R_{1(\text{silicon})} = \frac{.004}{(2.13) (.021 \times .021)} = 4.26 \text{ } ^\circ\text{C/W}$$

$$R_{2(\text{silicon})} = \frac{.002}{(2.13) (.025 \times .025)} = 1.50 \text{ } ^\circ\text{C/W}$$

$$\begin{aligned} R_{3(\text{epoxy})} &= \frac{.0015}{(.044) (.025 \times .025)} \\ &= 54.54 \end{aligned}$$

Add 10% for interface resistance:

$$54.54 + 5.45 = 59.99 \text{ } ^\circ\text{C/W}$$

$$R_{4(\text{gold})} = \frac{.0001}{(7.5) (.0251 \times .0251)} = 0.02 \text{ } ^\circ\text{C/W}$$

$$R_{5(\text{alumina})} = \frac{.025}{(.37) (.0502 \times .0502)} = 26.81 \text{ } ^\circ\text{C/W}$$

$$\begin{aligned} R_{6(\text{epoxy})} &= \frac{.003}{(.006) (.0752 \times .0752)} \\ &= 88.42 \end{aligned}$$

Add 10% for interface resistance:

$$88.42 + 8.84 = 97.26 \text{ } ^\circ\text{C/W}$$

Δ_1 Conductivity at 80°C (see Section 3.3).

3.1.1 (Cont.) Thermal Resistance

$$R_{7(\text{kovar})} = \frac{.020}{(.49)(.0952 \times .0952)} = 4.50 \text{ } ^\circ\text{C/W}$$

$$\text{The total resistance } R = 194.34 \text{ } ^\circ\text{C/W}$$

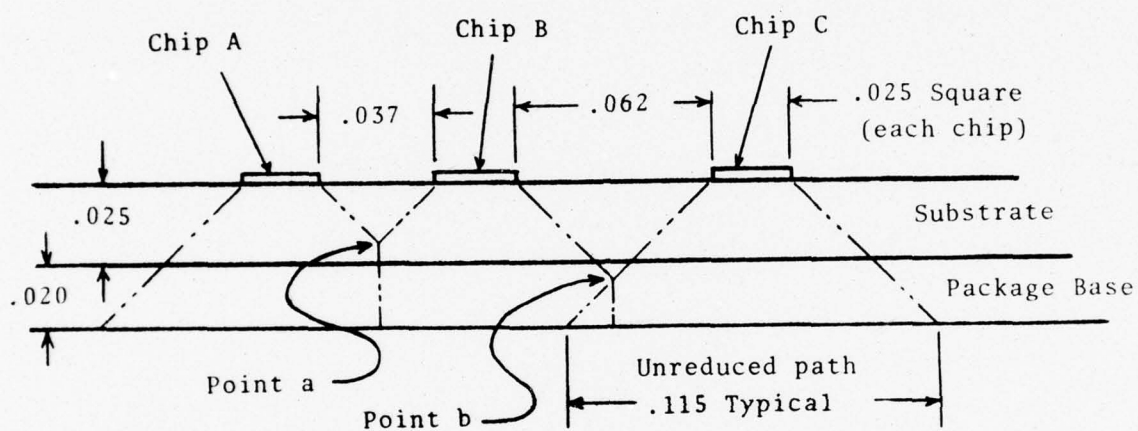
Note that the presumed thickness of 1-½ mils (.0381 mm) for the conductive epoxy under the chip is conservative. A thickness of 1 mil (.0254 mm) or less is more common. Note also that in spite of the fact that the conductive epoxy is only half the thickness and has seven times the conductivity of the non-conductive, its resistance is still 67% of that of the non-conductive epoxy. This is because the non-conductive epoxy has a larger cross section.

The percentage of resistance contributed by the thin gold mounting pad is so small, it is often ignored.

An important consideration is the effect on the heat-flow paths of two chips located relatively close to each other. If the heat-flow paths overlap, each is effectively reduced in area. The amount of influence on each other depends upon the power being dissipated by each chip. A complete analysis of such variables is beyond this text. However, a simplified and more conservative approach is as follows:

Assume that neither path overlaps the other but rather that the spreading of each one stops at the intersection point, and from that point on there is no further spreading of either path. Figure 3.1.1-3 illustrates this reduction of the heat flow paths.

3.1.1 (Cont.) Thermal Resistance



Assume no further heat spreading below intersection points a and b.
Dimensions shown are in inches.

Metric Equivalents

in.	mm
.020	.508
.025	.635
.037	.940
.062	1.575
.115	2.921

Figure 3.1.1-3 THERMAL MODEL OF ADJACENT CHIPS AND REDUCED HEAT-FLOW PATHS

3.1.1 (Cont.) Thermal Resistance

Figure 3.1.1-3 shows that for Chip A one side of the heat path is restricted, the other three sides continue to spread at 45 degrees. Because the heat path changes its shape within the thickness of the substrate, the resistance through the substrate should be calculated in two separate parts. The first part is from the top of the substrate down to the level of the intersection point with the path from Chip B. The second part is from the intersection point to the bottom of the substrate. Each part has its own mean-flow path. The heat paths through the epoxy and package are also restricted on one side. These also have modified heat paths. Figure 3.1.1-4 shows these modified paths and indicates the dimensions to be used for each portion.

With the exception of the first portion, the cross section of each portion is now a rectangle with unequal sides. The previous cross sections were all perfect squares.

If the chip in Figure 3.1.1-1 was in the position of Chip A in 3.1.1-3, then using the dimensions shown in Figure 3.1.1-4, the resistances through the substrate, epoxy and package could be recalculated as follows.

$$R_{5a}(\text{alumina}) = \frac{.0135}{(.37)(.0435 \times .0435)} = 26.42^{\circ}\text{C/W}$$

$$R_{5b}(\text{alumina}) = \frac{.0065}{(.37)(.0652 \times .0685)} = 3.93^{\circ}\text{C/W}$$

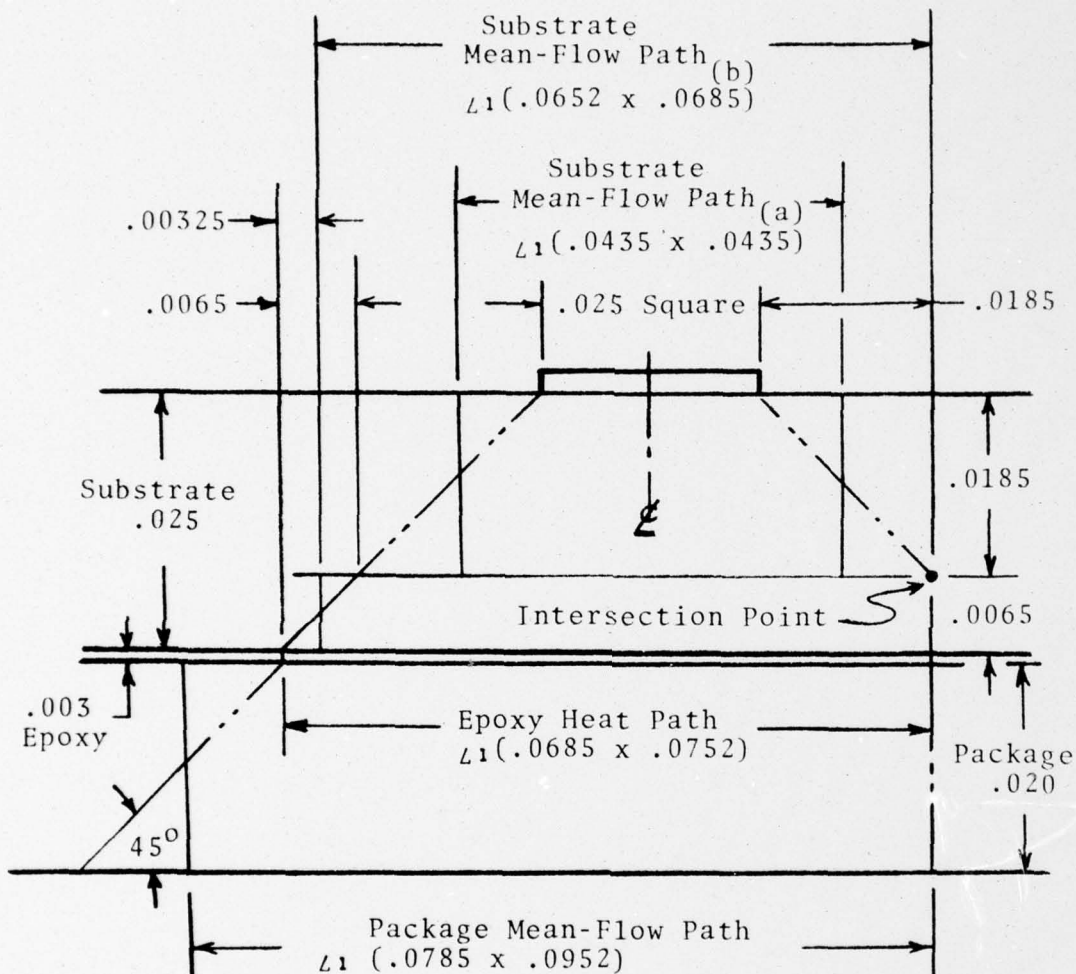
$$R_6(\text{epoxy}) = \frac{.003}{(.006)(.0685 \times .0752)} = 97.06^{\circ}\text{C/W}$$

$$\text{Add 10\% for interface resistance; } 97.06 + 9.706 = 106.77^{\circ}\text{C/W}$$

$$R_7(\text{kovar}) = \frac{.020}{(.47)(.0785 \times .0952)} = 5.46^{\circ}\text{C/W}$$

$$\text{The total resistance } R = 208.35^{\circ}\text{C/W}$$

3.1.1 (Cont.) Thermal Resistance



^{L1} In the dimensions for each heat path, the first dimension is the one shown in the sketch, the second is the dimension perpendicular to it.

Dimensions shown in the sketch are in inches.

Metric Equivalents		Metric Equivalents		Metric Equivalents	
in.	mm	in.	mm	in.	mm
.0030	.0762	.0200	.5080	.0685	1.7399
.00325	.0825	.0250	.6350	.0752	1.9101
.0065	.1651	.0435	1.1049	.0785	1.9939
.0185	.4699	.0652	1.6561	.0952	2.4181

Figure 3.1.1-4 MODIFIED HEAT PATHS FOR ADJACENT CHIPS

3.1.1 (Cont.) Thermal Resistance

Referring again to Figure 3.1.1-3, the reduction on one side of Chip B is the same as for Chip A. The other side of B would have no reduction through the substrate but only through the package base. Chip C would only have a reduced mean-flow path through the package base.

3.1.2 Temperature Rise

Assuming the chip in Figure 3.1.1-1 is dissipating 50 milliwatts, the calculation of the temperature rise is

$$\Delta T = 194.34^{\circ}\text{C/W} \times 0.05 \text{ W} = 9.7^{\circ}\text{C}$$

If the package case is at 100°C , the operating temperature of the chip element will be $\approx 110^{\circ}\text{C}$, which is below the common rating of 125°C for many silicon semiconductors.

Using the modified heat paths of Figure 3.1.1-4, the temperature rise is

$$\Delta T = 208.35^{\circ}\text{C/W} \times 0.05 \text{ W} = 10.4^{\circ}\text{C}$$

3.1.2 Temperature Rise

This would be an increase of only 0.7°C above that of the unreduced heat path. Such an increase is insignificant. However, when the heat path is reduced on more than one side, the influence can be important.

Referring to the resistance of Figure 3.1.1-1, it is worth noting the difference in temperature rise when substitutions are made for the epoxies. All other factors being equal, if solder were substituted for the conductive epoxy under the chip, the numbers would be

$$R_{3(\text{solder})} = \frac{.0015}{(1.08) (.025 \times .025)} = 2.22^{\circ}\text{C/W}$$

$$\text{Add 5\% for interface resistance; } 2.22 + .11 = 2.33^{\circ}\text{C/W}$$

$$\text{The total resistance } R = 136.68^{\circ}\text{C/W}$$

$$\Delta T = 6.83^{\circ}\text{C}$$

Substituting solder only under the substrate gives

$$R_{6(\text{solder})} = \frac{.003}{(1.08) (.0752 \times .0752)} = .49^{\circ}\text{C/W}$$

$$\text{Add 5\% for interface resistance } .49 + .024 = .514^{\circ}\text{C/W}$$

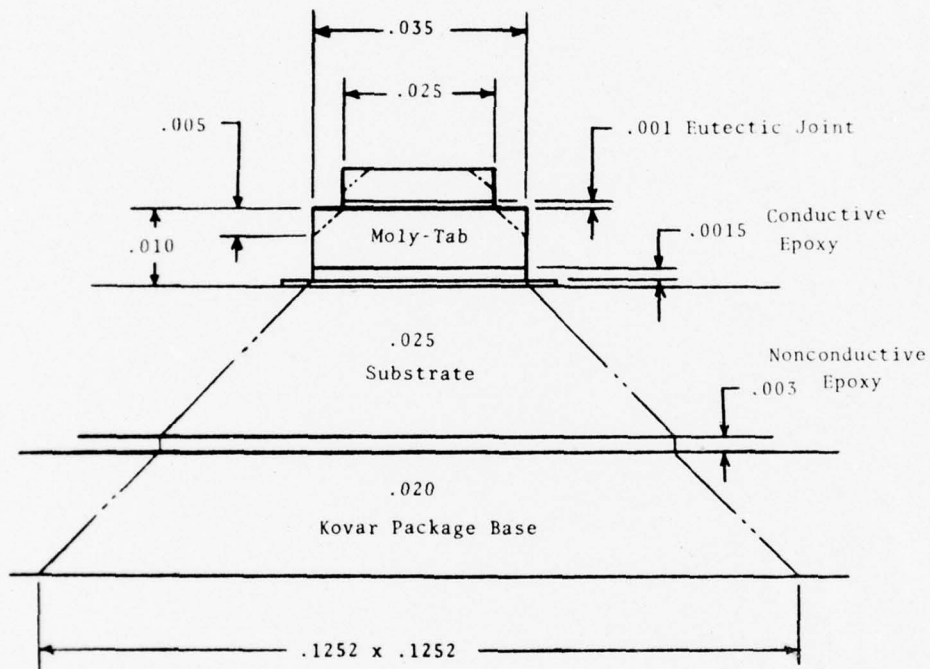
$$\text{The total resistance } R = 97.59^{\circ}\text{C/W}$$

$$\Delta T = 4.9^{\circ}\text{C}$$

It is clear that low conductivity material, even when the thickness is small, can make a significant difference.

3.1.2 (Cont.) Temperature Rise

Another comparison worth making is the difference created by eutectically attaching a chip to a "moly-tab" then epoxy-mounting the moly-tab on the substrate (a common practice when chips are high dissipators and require replacement).



Dimensions shown are in inches.

Metric Equivalent	
in.	mm
.0010	.025
.0015	.038
.0030	.076
.0050	.127
.0100	.254

Metric Equivalent	
in.	mm
.0200	.508
.0250	.635
.0350	.889
.1252	3.180

Figure 3.1.2-1 TYPICAL HEAT FLOW PATH WITH MOLY-TAB

3.1.2 (Cont.) Temperature Rise

The calculation of the temperature rise proceeds the same as before.

$$R_1(\text{silicon}) = \frac{.004}{(2.13)(.021 \times .021)} = 4.258 \text{ }^{\circ}\text{C/W}$$

$$R_2(\text{silicon}) = \frac{.002}{(2.13)(.025 \times .025)} = 1.502 \text{ }^{\circ}\text{C/W}$$

$$R_3(\text{eutectic}) = \frac{.001}{(7.5)(.025 \times .025)} = .213$$

Add 5% for interface resistance;

$$.213 + .011 = .224 \text{ }^{\circ}\text{C/W}$$

$$R_4(\text{molybdenum}) = \frac{.005}{(3.7)(.030 \times .030)} = 1.501 \text{ }^{\circ}\text{C/W}$$

$$R_5(\text{molybdenum}) = \frac{.005}{(3.7)(.035 \times .035)} = 1.103 \text{ }^{\circ}\text{C/W}$$

$$R_6(\text{epoxy}) = \frac{.0015}{(.044)(.035 \times .035)} = 27.83$$

Add 10% for interface resistance;

$$27.83 + 2.78 = 30.61 \text{ }^{\circ}\text{C/W}$$

$$R_7(\text{gold}) = \frac{.0001}{(7.5)(.0351 \times .0351)} = 0.01 \text{ }^{\circ}\text{C/W}$$

$$R_8(\text{alumina}) = \frac{.025}{(.37)(.0602 \times .0602)} = 18.64 \text{ }^{\circ}\text{C/W}$$

$$R_9(\text{epoxy}) = \frac{.003}{(.006)(.0852 \times .0852)} = 68.88$$

Add 10% for interface resistance;

$$68.88 + 6.88 = 75.76 \text{ }^{\circ}\text{C/W}$$

3.1.2 (Cont.) Temperature Rise

$$R_{10(\text{kovar})} = \frac{.020}{(.49)(.1052 \times .1052)} = 3.69 \text{ }^{\circ}\text{C/W}$$

The total resistance $R = 137.29 \text{ }^{\circ}\text{C/W}$

$$\Delta T = 6.86 \text{ }^{\circ}\text{C}$$

The 30% decrease in temperature rise using the moly-tab is achieved in spite of the fact that the heat path is longer. The spreading more than compensates for the longer heat path.

Note that the moly-tab was only 10 mils wider than the chip, and because of its 10 mil thickness, it did not take full advantage of the potential spreading. If surface space permits, the moly-tab size should take full advantage of the spreading (i.e., the difference in width between the moly-tab and the chip should be twice the moly-tab thickness).

3.2 BEAM LEAD ANALYSIS

The heat flow path that conducts the heat away from an inverted beam-leaded chip is divided into the several parallel paths formed by the leads themselves. The calculation of the resistance through those paths is the same as the calculation of electrical resistances in parallel. The inverse of the total resistance is equal to the sum of the inverses of the individual resistances.

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} - - -$$

where $R = \text{Total resistance}$

$R_1, R_2, \text{ et al} = \text{Resistances of the individual beams}$

3.2 (Cont.) BEAM LEAD ANALYSIS

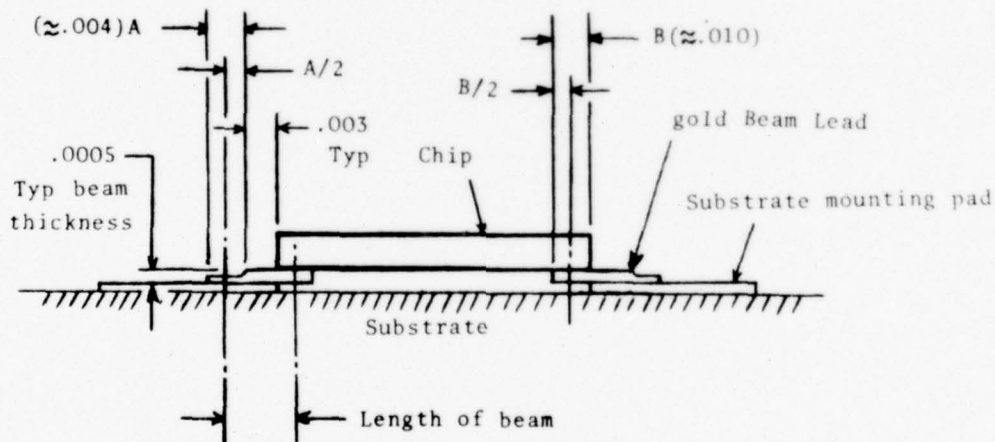
The resistance through an individual beam is calculated as a heat flow path having a constant cross section, since there will be no heat spreading throughout the length of the beam.

$$R_1 = \frac{\text{Length}}{(\text{Conductivity})(\text{Cross Sectional Area})}$$

Gold is the most common beam lead material.

For the cross-sectional area, use the undeformed cross-sectional area of the beam.

The length can be taken as shown in Figure 3.2-1.



Dimensions given in inches.

Metric Equivalent	
in.	mm
.0005	.0127
.0030	.0762
.0040	.1016
.0100	.2540

Figure 3.2-1 LENGTH OF BEAM LEAD

3.2 (Cont.) BEAM LEAD ANALYSIS

$$\text{For a single beam } R_1 = \frac{.010}{(7.5)(.0005 \times .004)} = 666.66^{\circ}\text{C/W}$$

Assuming equal heat distribution through sixteen beams, the total resistance is:

$$\frac{1}{R} = \frac{16}{666.66}; \quad R = 41.66^{\circ}\text{C/W}$$

The heat flow paths that spread from the beams through the substrate describe complex overlapping patterns due to the close proximity of the beams to each other. A simplified model of the paths through the substrate is depicted in Figure 3.2-2. The model shows no overlap between any of the adjacent paths. This is a conservative approach, and the calculations will indicate high resistances. Designs that can pass such stringent appraisal should have adequate heat transfer.

In Figure 3.2-2, the mean flow cross-sectional area for an individual heat path would be: .010 x .029.

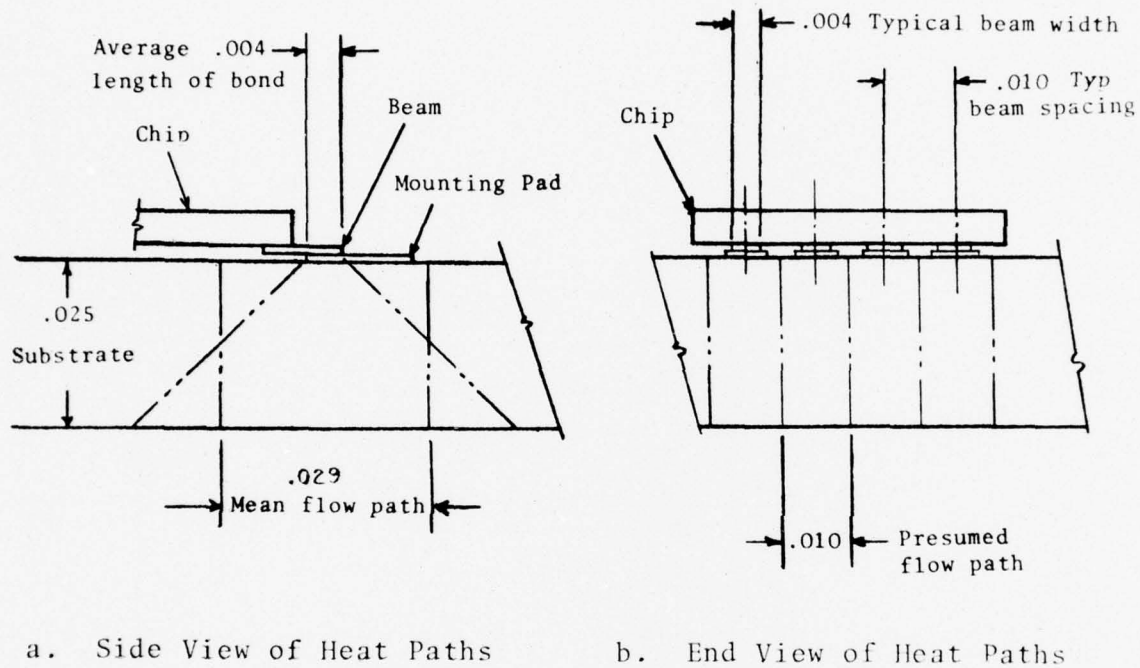
Each individual resistance would be:

$$R_{1(\text{alumina})} = \frac{.025}{(.37)(.010 \times .029)} = 232.99^{\circ}\text{C/W}$$

If the chip has sixteen beams, the total resistance through the substrate would be:

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \dots + \frac{1}{R_{16}}$$

3.2 (Cont.) BEAM LEAD ANALYSIS



Dimensions are in inches.

Metric Equivalents

in.	mm
.004	.102
.010	.254
.025	.635
.029	.737

Figure 3.2-2 BEAM LEAD HEAT PATHS THROUGH SUBSTRATE

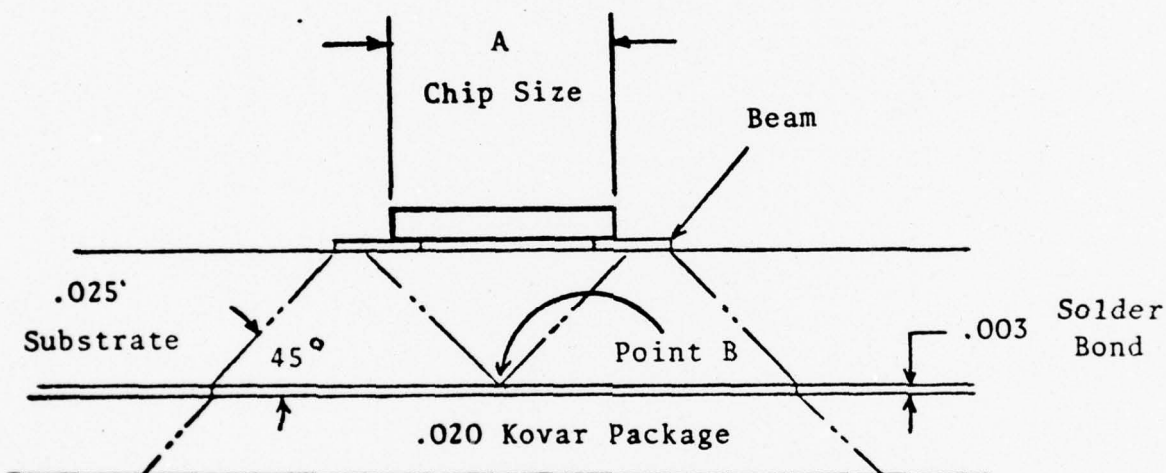
Continuing the assumption that each of the sixteen paths carries the heat equally, the total will be:

$$\frac{1}{R_{\text{alumina}}} = \frac{16}{232.99} ;$$

$$R_{\text{alumina}} = 14.56^{\circ}\text{C/W}$$

3.2 (Cont.) BEAM LEAD ANALYSIS

The resistance through the package base can often be treated as a single heat path, since the heat reaching the package is uniformly distributed over the area (due to the spreading through the substrate). However, for a large chip the spreading through the substrate may not cover the entire area under the chip. Figure 3.2-3 illustrates how the chip size affects the heat path through the substrate and package base.



Note: The location of point B is determined by chip size "A".

Figure 3.2-3 CHIP SIZE VERSUS HEAT PATH THROUGH SUBSTRATE AND PACKAGE

The heat paths shown converging at point B (bottom of substrate) describe an ideal configuration (no overlap of the paths through the substrate and a single path through the package base). Obviously, the chip size (dimension A) determines the location of point B. In the configuration shown, the chip dimension A would need to be .044 in. (1.118 mm). For a chip larger than

3.2 (Cont.) BEAM LEAD ANALYSIS

.090 in. (2.286 mm), point B would be below the package base. Figure 3.2-4 shows the case for which the point B_1 is above the bottom of the substrate. The heat path through the substrate should be divided into three parts, two parallel paths having lengths down to point B_1 , and the third path from B_1 to the bottom of the substrate. Figure 3.2-4 shows the three mean-flow paths. (The concept is the same as previously used in Figure 3.1.1-4 for adjacent chips.)

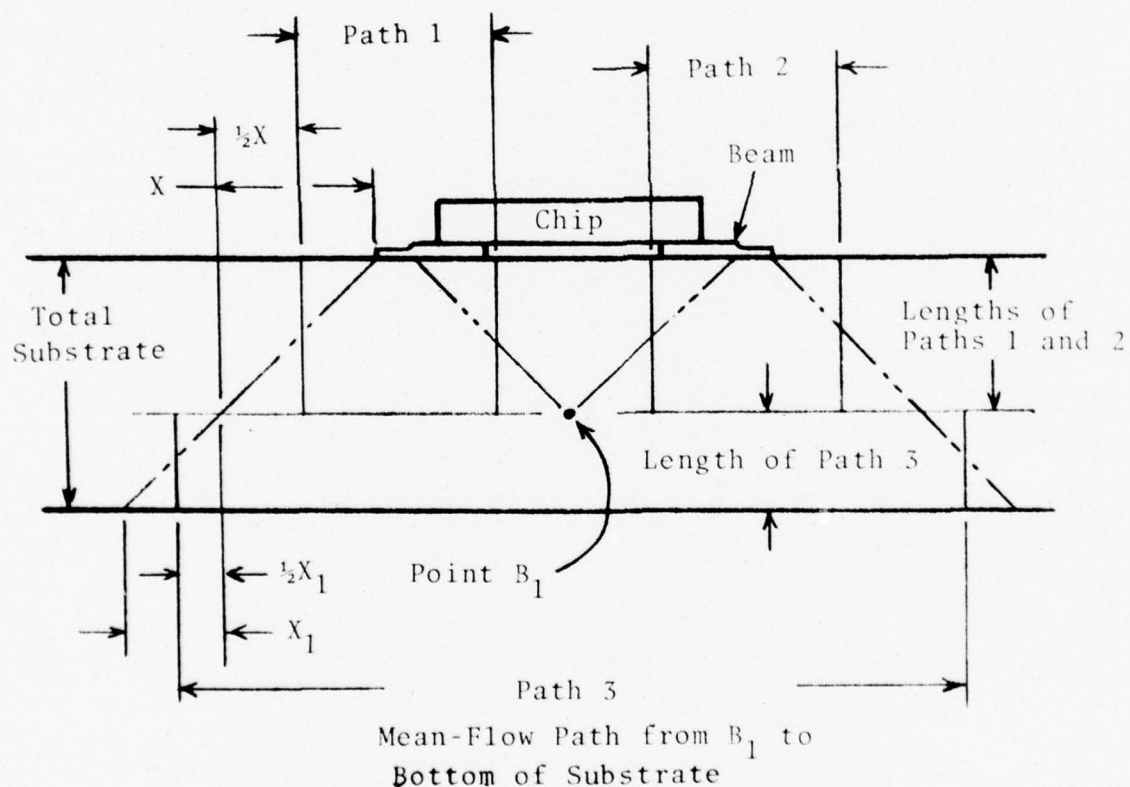


Figure 3.2-4 MODIFIED MEAN-FLOW PATHS FOR BEAM-LEADED CHIPS

3.2 (Cont.) BEAM LEAD ANALYSIS

If the point B_1 was below the substrate but within the thickness of the package, modified heat paths would be used for only the package.

As previously stated, to create the idealized configuration in Figure 3.2-3, the chip size would be .044. Continuing that assumption, the resistances through the solder and kovar package are

$$R_{(\text{solder})} = \frac{.003}{(1.08)(.108 \times .108)} = .238^{\circ}\text{C/W}$$

Add 5% for interface resistance; $.238 + .012 = .250^{\circ}\text{C/W}$

$$R_{(\text{kovar})} = \frac{.020}{(.49)(.128 \times .128)} = 2.49^{\circ}\text{C/W}$$

The total resistance, $R = 58.96^{\circ}\text{C/W}$

Dissipating 100 milliwatts, the chip would see a temperature rise of 5.9°C above the package surface temperature.

3.3 THERMAL CONDUCTIVITY OF VARIOUS MATERIALS

The conductivity figures quoted in the following chart (Table 3.3-1) were compiled from handbooks, manufacturer's catalogs, and from empirical evaluation. None of the figures should supersede more specific data pertaining to material being used in a particular design.

3.3 (Cont.) THERMAL CONDUCTIVITY OF VARIOUS MATERIALS

Two units are given. The W/in.^{°C} is most suitable for this text, and the Btu/hr ft^{°F} is a unit commonly quoted in handbooks and by material manufacturers. A units-conversion chart (Table 3.3-2) is provided later in this section. The chart gives conversion factors for several different units.

Table 3.3-1 THERMAL CONDUCTIVITIES OF VARIOUS MATERIALS

Material	Thermal Conductivity at 25°C	
	W/(in) (°C)	Btu/(hr) (ft) (°F)
Silver	10.6	241
Copper	9.6	220
Eutectic Bond	7.5	171
Gold	7.5	171
Ⓐ Beryllia 99.5%	6.25	143
Ⓐ Beryllia 98%	5.25	120
Aluminum Alloy	4.38	100
Molybdenum	3.7	84
Nickel	2.1	48
Silicon	2.13	48.5
Tin	1.54	35.3
Solder: (% Composition)		
80 Indium, 15 Pb, 5 Ag	1.09	24.88
60 Pb, 40 Sn	1.08	24.65
Lead	0.87	20
Ⓐ Alumina (99.5%)	0.74	17
Ⓐ Alumina (96%)	0.44	10
Ⓐ Kovar (Ni Co Fe)	0.49	11.2
Ⓐ Kovar (Ni Fe)	0.34	7.7
Epoxy (BeO filled)	0.088	2.0
Conductive Epoxy (Ag)	0.044	1.00
Borosilicate Glass	0.026	0.59
Glass Frit	0.024	0.57
NonConductive Epoxy:		
(Alumina Filled)	0.020	0.47
(Non Filled)	0.006	0.15
Epoxy Glass Laminate	0.007	0.17
Silicon RTV (Unfilled)	0.004	0.10

Ⓐ The name "kovar" has been used for two different metallic compositions. One is 29% nickel, 17% cobalt, 54% iron. The other is 50% nickel and 50% iron.

Ⓐ The conductivities of beryllia (BeO) and alumina (Al₂O₃) vary significantly as the material temperature varies.

3.3 (Cont.) THERMAL CONDUCTIVITY OF VARIOUS MATERIALS

Although it is a fact that the ability of any material to transfer heat does vary as the material temperature varies, for most materials shown here, this variation is not significant over the temperature range in which most hybrids operate. Exceptions are the ceramic materials, alumina and beryllia. Therefore, a graph is provided in Figures 3.3-1, showing conductivity variations for certain manufacturer's ceramics.

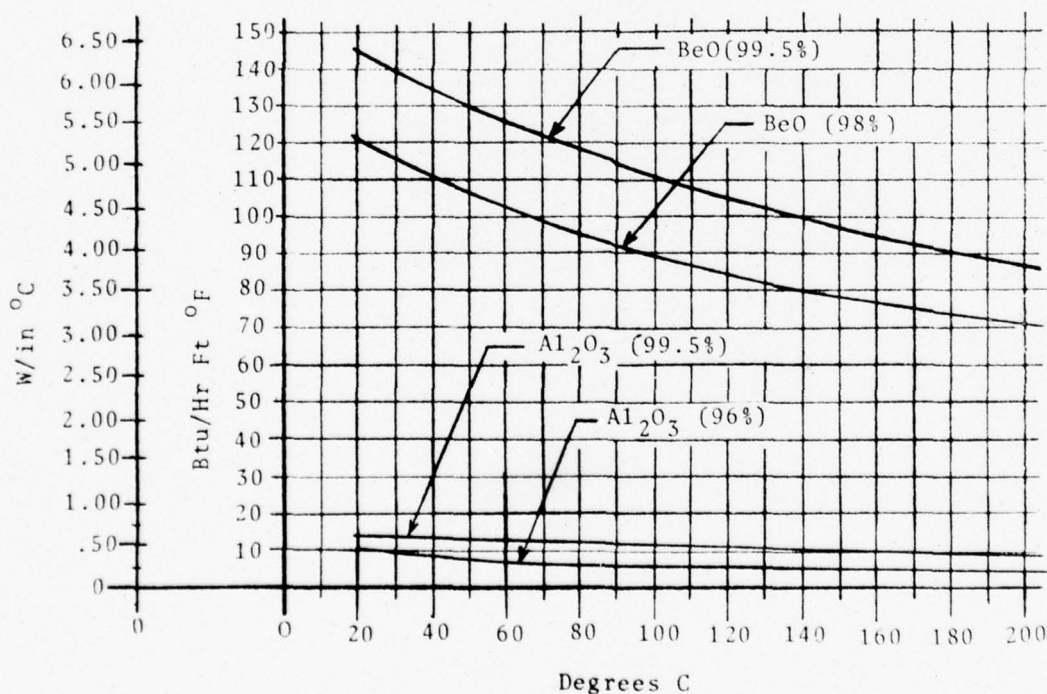


Figure 3.3-1 CONDUCTIVITY VARIATIONS OF Al_2O_3 AND BeO

3.3 (Cont.) THERMAL CONDUCTIVITY OF VARIOUS MATERIALS

Table 3.3-2 lists factors for converting various thermal conductivity units. To convert from a unit in the left column to one of the units listed across the top, multiply by the factor shown within the matrix.

Table 3.3-2 THERMAL CONDUCTIVITY UNITS CONVERSION FACTORS

FROM	TO			
	$\frac{\text{Cal}}{(\text{s})(\text{cm})(^{\circ}\text{C})}$	$\frac{\text{W}}{(\text{cm})(^{\circ}\text{C})}$	$\frac{\text{W}}{(\text{in})(^{\circ}\text{C})}$	$\frac{\text{Btu}}{(\text{hr})(\text{ft})(^{\circ}\text{F})}$
$\frac{\text{Cal}}{(\text{s})(\text{cm})(^{\circ}\text{C})}$	1	4.18	10.62	241.9
$\frac{\text{W}}{(\text{cm})(^{\circ}\text{C})}$	2.39×10^{-1}	1	2.54	57.8
$\frac{\text{W}}{(\text{in})(^{\circ}\text{C})}$	9.43×10^{-2}	3.93×10^{-1}	1	22.83
$\frac{\text{Btu}}{(\text{hr})(\text{ft})(^{\circ}\text{F})}$	4.13×10^{-3}	1.73×10^{-2}	4.38×10^{-2}	1

SECTION 4 ELECTRICAL TESTS

The testing of hybrids differs from testing of discrete circuit assemblies in three noticeable ways: (1) checkout of a multi-layer substrate is a necessary expenditure; (2) due to less pretesting of naked semiconductors, there is the potential for finding more component failures during testing; and (3) extra care must be exercised when using probes to make electrical contact inside the hybrid.

4.1 FUNCTIONAL INTEGRITY

Because its small size is the most obvious feature of a hybrid, there is a temptation to fill each package to its limit. This tendency has in the past been carried to the extreme of putting a portion of one functional unit into a package with another circuit that had extra space, and the remainder into another. While this can reduce the number of packages, testing such separated circuits can be very clumsy, time consuming, and accumulated errors may go undetected.

Another factor is that one unit cannot be scheduled independently through manufacturing and test. If one such partial circuit reached the testing stage before the remainder, the testing would have to wait until all parts were available. Failures and rework of one part can delay shipment of several parts. Testing a unit as an independently-functional entity is paramount to the efficiency of the testing and the work flow.

4.2 FAULT ISOLATION

After the cover has been sealed, a hybrid can withstand severe stresses; but before the cover is sealed, the fragility of the exposed circuit elements makes them susceptible to damage. Every factor that increases the need to probe inside the hybrid increases the risk of damage.

One such factor is that naked semiconductors typically receive only minimal pretesting, thereby increasing the potential for faulty components to be discovered in test. The need to isolate the faulty component increases the need to probe. Another factor is that the number of times a particular component can be removed and replaced is limited, and each rework cycle risks damage to all the circuit elements. These facts emphasize the need to accurately determine the faulty element before rework is ordered. This need to be accurate usually requires more probing than might be needed to make an educated guess.

Besides mechanical damage, probing can be deleterious in yet another way. The cover must be off the hybrid in order to probe. The longer the package is open, the greater the risk of moisture or other contaminants getting inside. Applying an electrical stimulus with certain contaminants present may even increase the deterioration.

The need to diminish these risks should influence the design phase of the hybrid. The responsible test engineer should be consulted before the layout design begins, and should pass judgment on the layout when it is completed. Whenever possible, extra pins in the package should be used to provide test points outside the package. Where potential probe points must be on the substrate, adequate clearance should be provided around each such point.

4.2 (Cont.) FAULT ISOLATION

If a multilayer design is used, fault isolation can be significantly simplified by providing various arrangements of standard test point patterns on the substrate. One such standard is a pattern of test points for each substrate size, only one multiple-probe assembly is required for each size. The probe assembly can be optically or mechanically aligned before being lowered to contact the substrate. Such a system, compared to moving a single probe from point to point, greatly improves the testing efficiency and reduces the risk of damage. (The same probes might also be used to check out the multilayer substrate before it is used in the hybrid.)

Another such standard for use with I.C. chips is to establish a few wire-bonding patterns to be used with any chip according to the number of terminals on the chip. Each substrate pad is extended to provide not only a bond point but also a probe point. One multiple probe assembly can be available for each such pattern. Fault isolation can then be accomplished by using the appropriate multiple-probe to test each chip individually.

If a computer is available for use in testing, it can significantly reduce the amount of probing required. The computer can be programmed to not only recognize failures but also to logically determine the most probable failure point internal to the package. It can do this while contacting only the output leads of the package.

Of course, the best way to reduce the fault isolation procedures is to reduce the number of faulty components by pretesting. Semiconductors can be mounted in chip carriers and pretested prior to being mounted on the substrate. These carriers do consume a

4.2 (Cont.) FAULT ISOLATION

large area on the substrate, and additional manufacturing processes are required, but they are definitely worth consideration, because pretesting the chips diminishes the chain of potential problems at its source.

Electrical testing is a major portion of the cost and time expended for a hybrid. Fault isolation can be a major portion of that testing. The methods mentioned, and any other methods that reduce the need or simplify the procedure for isolating failures, are worth consideration.

4.3 MULTILAYER SUBSTRATE CHECK-OUT

After a multilayer substrate has been fabricated, it is necessary to ascertain whether there are electrical shorts or open connections hidden below the dielectric material or within the vias.

It is not sufficient to check only the continuity of each conductor track. Proof is required that no connection exists between any two tracks that cross each other if the two are separated by only one layer of dielectric material. (Double printing and firing the dielectric greatly reduces such shorts but it is no guarantee.)

Each point to be probed must be assigned a designation, then a list must be generated that describes which points must be connected and which ones require proof of no connection. (Such a list is described in Section 9.9.) Using a check-out list and two hand-held probes, the substrate can be manually probed at each of the designated points. A connection between two points is typically indicated by a light or buzzer. Manual check-out of a multilayer substrate can be very time consuming. The testing of 300 points can take up to 2 hours. The operator must consult the check-out list, then the drawing that shows the location of each designated point, then she must find that point on the substrate in order to place each probe. One procedure that can save time is to have the list read onto a recording tape then play the tape to the operator through earphones. If the tape player is provided with a foot actuated switch, the operator can advance the tape at will. In some cases, after good yields have been consistently achieved, the check-out procedure is performed on only a sample quantity from each lot.

4.3 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT

Automatic equipment can be used to perform these tests. For automatic check-out, multiple probes make contact to all the probe points simultaneously. The probes are wired through a harness to connectors that are plugged into the automatic equipment. The equipment compares each point to every other point. Automatic equipment using relay switching can check-out 300 points in approximately 5 minutes. Solid state equipment can operate faster.

There are vendors who specialize in producing custom multiple-probe assemblies (usually mounted on printed circuit boards). Such a custom assembly, however, is suitable for only one substrate. Another technique is to design the substrate to have standard locations for all probe points. In this case one probe assembly can be used universally. One such standardization scheme locates I.C. chips in a matrix of rows and columns. The wire bonding pads surrounding each chip fan out in a sunburst pattern and terminate in enlarged pads that serve as the probe points. These probe pads plus the standard exit pads along the edges of the substrate will provide all the probe points necessary if every substrate conductor track is connected to one of these points. If every conductor track is not required by the schematic to be connected to one of the standard probe points, the unconnected conductors can often be arbitrarily connected to the probe points. After checkout, these arbitrary connections can be cut open by using a programmable laser trimmer or by manipulating the substrate with a pantograph linkage while the laser cuts the tracks.

Automatic equipment used for continuity check-out is usually programmable so that each point-to-point connection is compared to the required connection in the program. Errors in connections

4.3 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT

can be recorded on a print-out if the machine has such a printer. For the first several substrates of a new design, it is advisable to have the check-out machine proceed through the entire check list rather than stopping at the first error. If the same failure repeats on several substrates, this may indicate a defect in the thick film screen.

Some automatic equipment can generate its own program tape. The probes are applied to a substrate known to be correct, and the machine "reads" the connections and creates the tape to match those connections. Such automatic programming requires manual check-out, of course, in order to find the substrate known to be correct.

SECTION 5 COMPONENTS AND MATERIALS

This section describes some of the components and materials commonly used in hybrids. Various configurations of packages are shown and the range of sizes is indicated. Substrate shapes are shown to make clear that any shape can be fabricated. Examples of semiconductor configurations show the commonly used metal-lization patterns for diodes and transistors. Resistor and capacitor chips are shown with size and value ranges indicated. Information is also included about solders, epoxies, and inter-connecting wires.

5.1 PACKAGES AND COVERS

For military and space applications, metal packages and metal covers are most frequently used, but ceramic packages and covers are not uncommon.

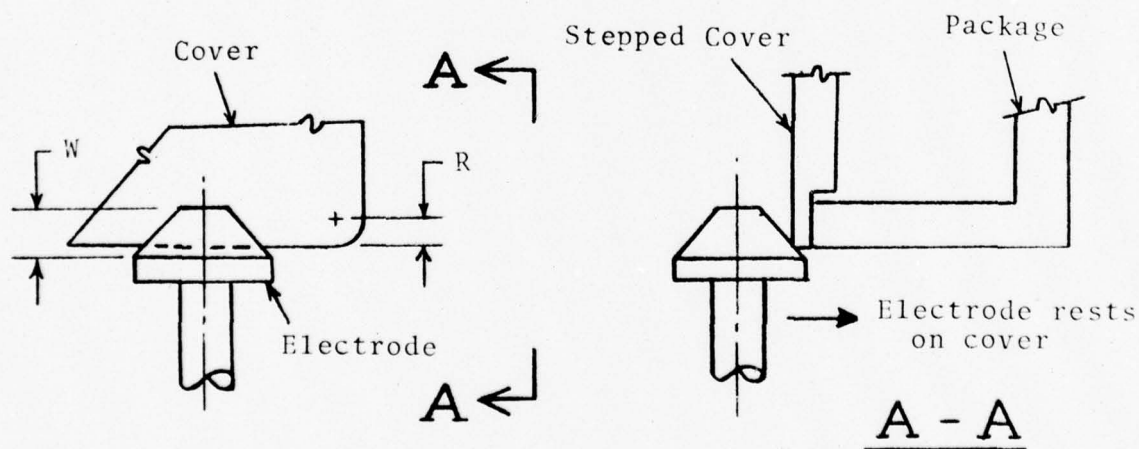
The metal packages are rugged and can provide electrostatic shielding. Kovar is the metal most frequently used because its coefficient of thermal expansion is closely matched to certain glass materials and these glasses are used to seal around the package leads. Kovar is however much heavier than ceramic, so a weight penalty must be paid to obtain the other desirable features. If the ceramic package is high purity alumina, it has a slight advantage over kovar when comparing their respective thermal conductivities.

Beryllia ceramic has more than ten times the thermal conductivity of kovar. Beryllia, however, is expensive and the handling (particular high temperature processes) requires safety precautions because the material is toxic.

5.1 (Cont.) PACKAGES AND COVERS

When a flat cover is to be used to weld-seal a package, the corners of the package need special attention. Because the welding electrodes pass along each edge separately, a large radius in the corner will leave a portion untouched by the electrodes and the seal will not be continuous around the radiused corners. The radius in each corner should be less than the width of the working face of the electrode. Figure 5.1-1 shows the relationship of the package corner radius to the width of the welding electrode.

The weld-sealing process works best on a cover thickness of approximately 5 mils (0.127 mm), but in medium or large sizes the thickness should be at least 10 mils (0.254 mm) for sufficient rigidity. (For very small sized packages 5 mils might be sufficient.) A compromise between the two requirements is to use a cover that is 10 mils or more but is cut down to 5 mils thickness only along the edges. Such a cover is called a "stepped cover".

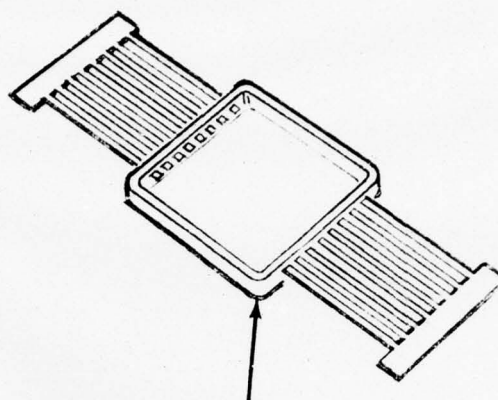
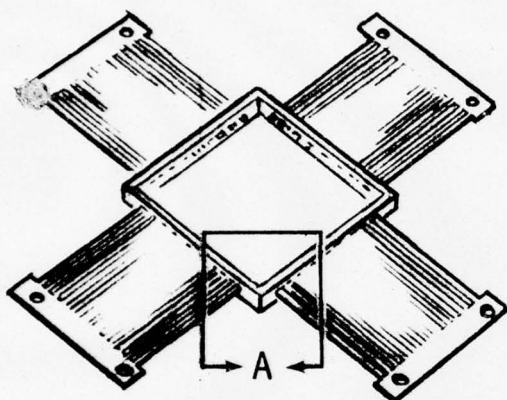


Radius (R) should be less than width (W) of the working face of the electrode.

Figure 5.1-1 PACKAGE CORNER RADIUS VERSUS WIDTH OF WELDING ELECTRODE

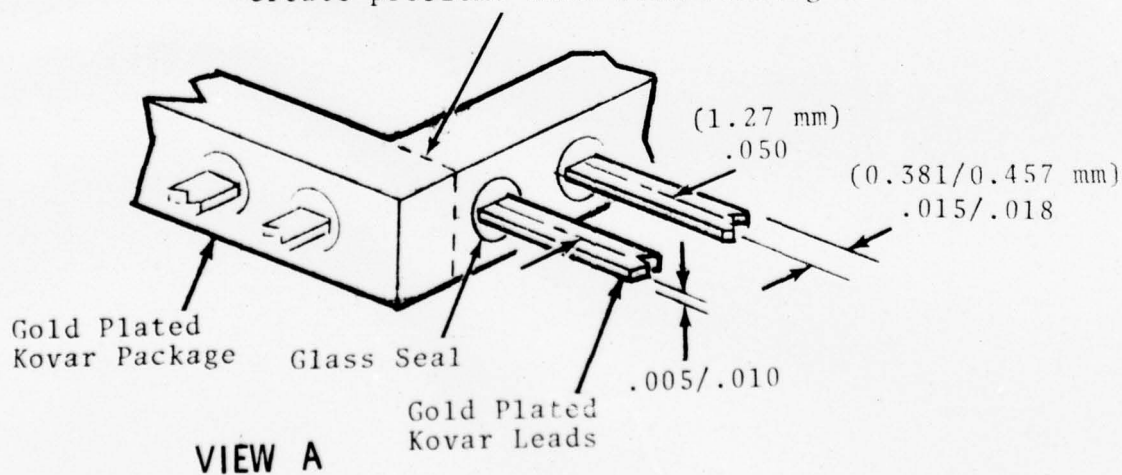
5.1 (Cont.) PACKAGES AND COVERS

Butterfly Packages

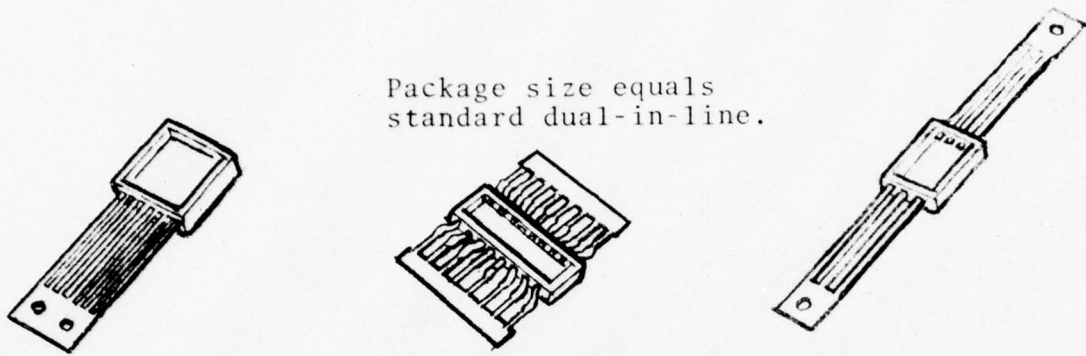


Available with sharp
or radiused corners

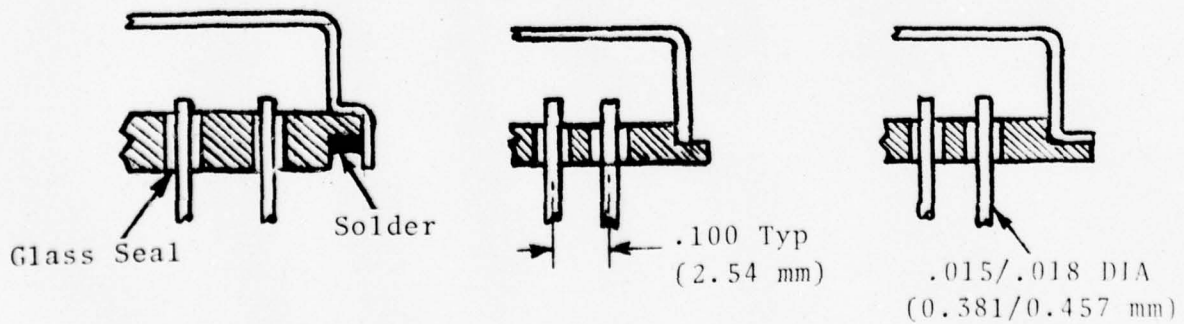
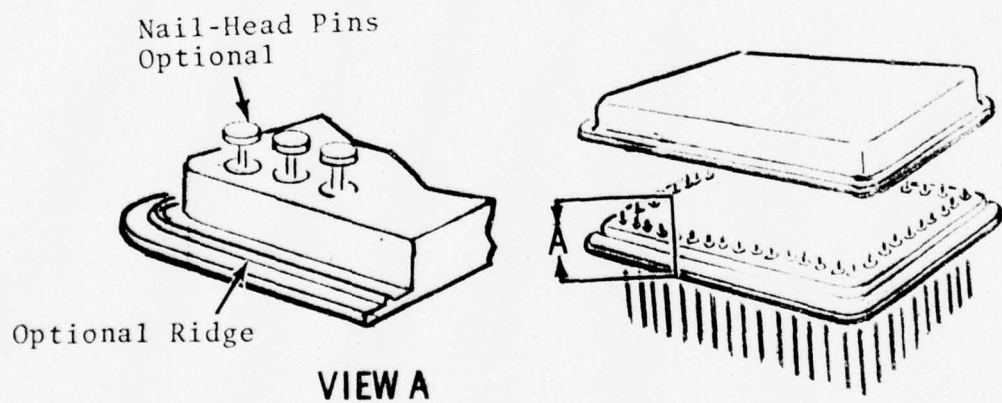
Side walls sometimes made from separate,
brazed-together pieces. Joint might
create problems when weld-sealing cover.



5.1 (Cont.) PACKAGES AND COVERS

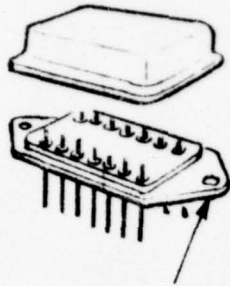


Platform Packages

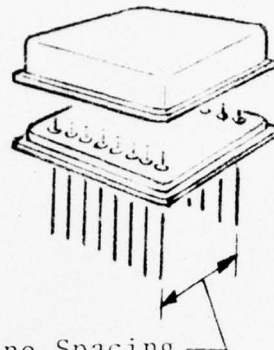


Various Cover and Platform Combinations

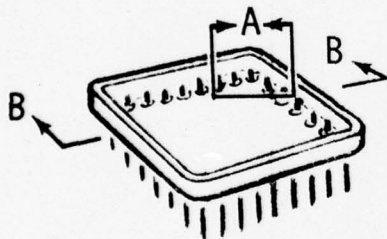
5.1 (Cont.) PACKAGES AND COVERS



Flange provides good heat sink mounting



Dual-In-Line Spacing



Nail-Head Pins Optional

Gold Plated Kovar Package

Glass Seal

VIEW A



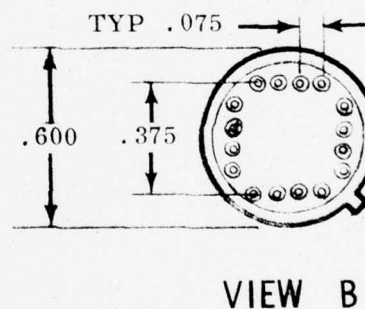
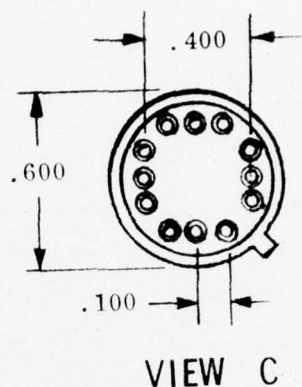
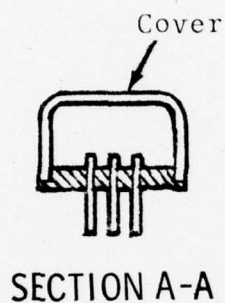
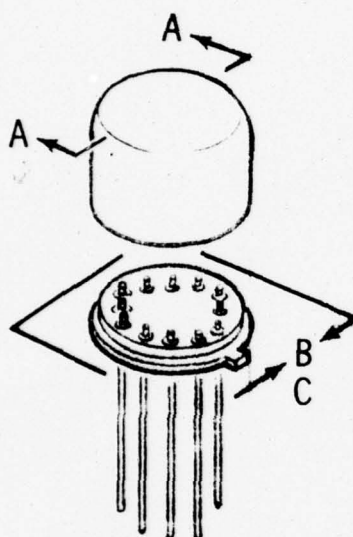
Double Row of Pins Each Side

.100 TYP
(0.254 mm)

SECTION B-B

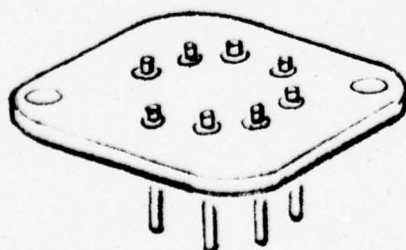
5.1 (Cont.) PACKAGES AND COVERS

TO-8 PACKAGES

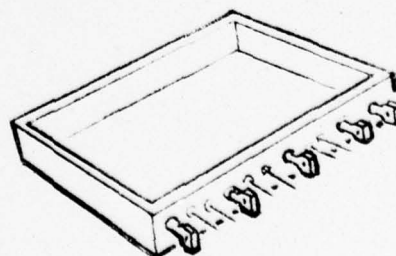


Various Pin Patterns

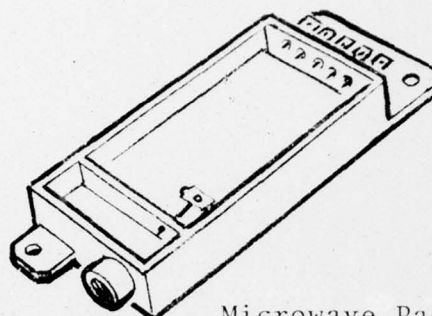
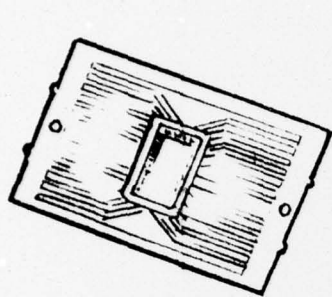
TO-3 Package



High Power Package

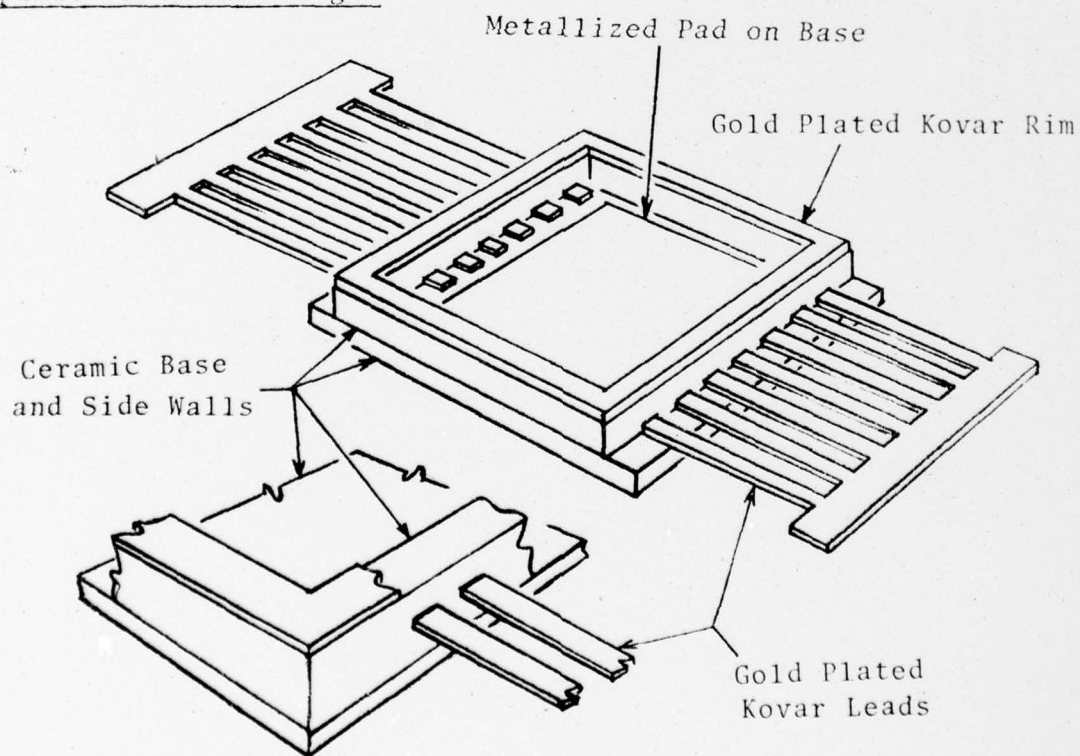


5.1 (Cont.) PACKAGES AND COVERS



Microwave Package

Typical Ceramic Packages



5.1 (Cont.) PACKAGES AND COVERS

Package sizes range from 0.25 x 0.25 in. (6.35 mm) to 2.50 x 2.50 in. (63.5 mm), with leads on one, two, three, or four sides. The number of leads ranges from 6 to 120. (120 leads on 2.00 x 2.00 in. butterfly package.) (110 leads are available on a 2.00 x 1.00 in. butterfly package.) The package can have one pin connected to package; also one pin with a color coded glass seal to indicate pin orientation. Butterfly packages can have round leads, and platform packages can have flat leads.

For flat leads, the most common spacing is 50 mils (1.27 mm) center to center; round leads in plug-in style flat packages are typically on 100 mils (2.54 mm) centers.

TO-8 packages can have extended leads on the top side to accommodate several substrates being staked and soldered on the leads. Extra high covers can be used with these extended leads. (This packaging method places a heavy emphasis on pretesting the substrates before installation, because lower substrates are inaccessible.)

The side walls with sealed leads typically used in a butterfly style package can be obtained without the package base. These assemblies can later be mounted on whichever base is chosen. They are sometimes used when the substrate itself will form the package base.

5.2 SUBSTRATES

Substrates are available in many shapes and sizes, and with the exception of rectangular shapes, they are usually made to fit a particular package configuration. Substrates can be custom made

5.2 (Cont.) SUBSTRATES

to almost any shape. When the ceramic is in the "green state" (unfired), irregular shapes can be punched using a tool similar to a cookie cutter. However, flatness is more difficult to maintain when the size is large or the shape is irregular. (Most manufacturers specify standard camber of 4 mils per inch of length (up to 2 inches (50.8 mm).) If the camber of the as-fired ceramic is too large, the surface can be ground to whatever flatness is required, but this makes a large difference in the cost of the substrate. Holes can be added to a ceramic substrate after it has been fired, but again this is a costly process.

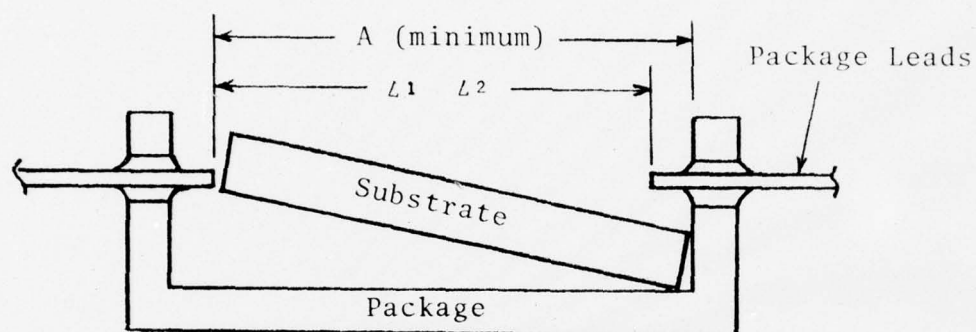
Substrates are commonly used in thicknesses from 10 mils (0.254 mm) to 50 mils (1.27 mm). Rectangular shapes are available in many combinations of dimensions.

Substrates can also be purchased with scribe lines already cut into the surface. These prescribed substrates are usually intended to accommodate a matrix of step-and-repeated image patterns. After processing, the substrate need only be broken; the scribe lines are already there. When using prescribed substrates it is important to determine the maximum width of the scribed line so that this width can be taken into account in the step-and-repeat dimensions. Prescribed substrates can be ordered to custom dimensions. (Ceramic chip resistors are often fabricated on prescribed substrates.)

Usually the specifications for a butterfly type package will indicate the maximum size substrate allowable. If that information is not available the substrate dimensions can be determined from the dimensions of the package. When making such a determination the tolerances of the package dimensions must be taken into account.

5.2 (Cont.) SUBSTRATES

For a package with leads on two sides, the maximum substrate dimension in relation to the leads can be determined as shown in Figure 5.2-1.



The minimum dimension of A dictates the maximum dimension of the substrate.

Figure 5.2-1 SUBSTRATE DIMENSION RELATED TO PACKAGE LEADS

- L1** For a package with leads on four sides the relationship shown in Figure 5.2-1 is only applicable to one substrate dimension. The other (maximum) substrate dimension must be less than the minimum distance between the leads.
- L2** If components and wires are to be on the substrate before it is installed into the package, and if damage might be caused by placing the substrate under the package leads (as shown), then the maximum substrate dimension should be less than the minimum distance between the leads so that the substrate can pass horizontally between the leads.

Holes in ceramic substrates can be metallized on the inside edge of the holes (similar to plated-through holes in a PC board).

5.2 (Cont.) SUBSTRATES

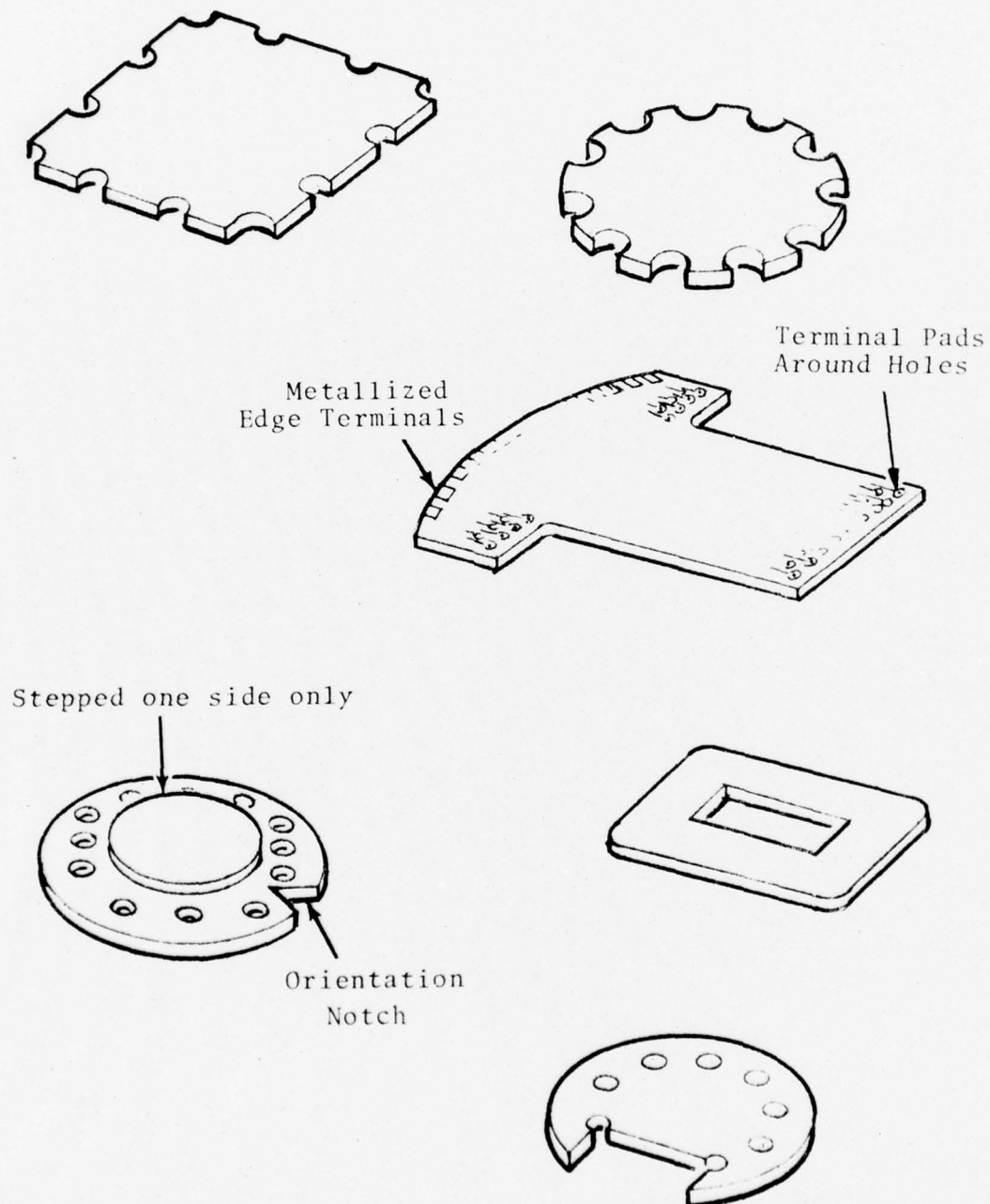
High purity, small grain ceramics are available with as-fired (unglazed) surface roughnesses $<10 \mu$ in. suitable for thin film applications. Thick film materials adhere best with slightly rougher surfaces.

Some examples of ceramic properties are shown below.

PROPERTIES	UNITS	ALUMINA		BERYLLIA
		96%	99.5%	99.5%
Water Absorption	%	0	0	0
Flexural Strength	PSI	46,000	70,000	53,000
Dielectric Strength @ 60 HzAC (Test Disc .25 in. (6.35 mm) Thick)	Volts Per Mil	210	^{L1} 220	230
Volume Resistivity: 25°C 100°C	Ω cm	$>10^{14}$ 2×10^{15}	$>10^{14}$ 7×10^{13}	$>10^{14}$ $>10^{14}$
Dielectric Constant: 1 MHz 10 GHz		(25°C) 9.3 9.2	(25°C) 9.9 9.8	(25°C) 6.9 6.8

^{L1} 700 @ .025 in. (.635 mm) thick.

5.2 (Cont.) SUBSTRATES



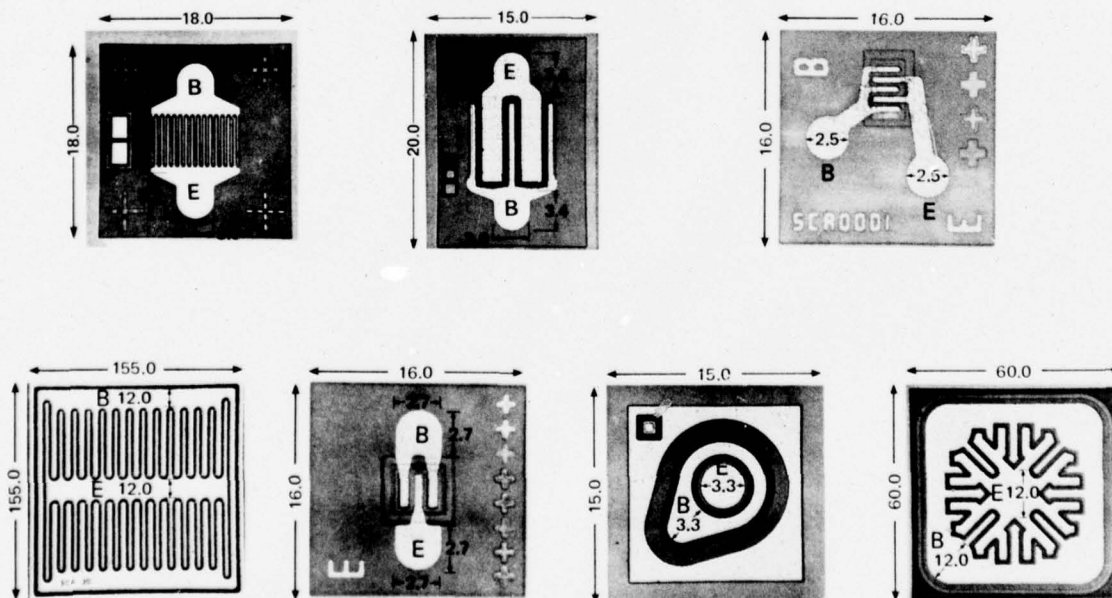
5.3 SEMICONDUCTORS

Almost any semiconductor device can be purchased as a naked chip. Many can be purchased in wafer form (unsliced) at significant cost reductions. (These would, of course, require "dicing" later.) As an example of availability, included is a copy of one vendor's catalog listing of available chips. When ordering any semiconductor, the requirement for back side gold metallization should be indicated.

The following are examples of semiconductor chips and some of the typical metallization patterns used.

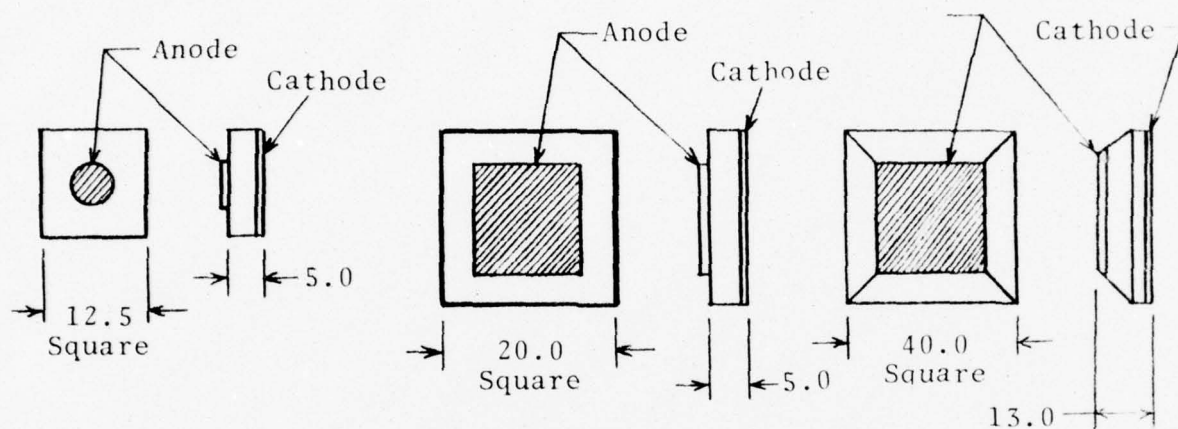
Typical Transistor Configurations

(Dimensions shown are mils.)



5.3 (cont.) SEMICONDUCTORS

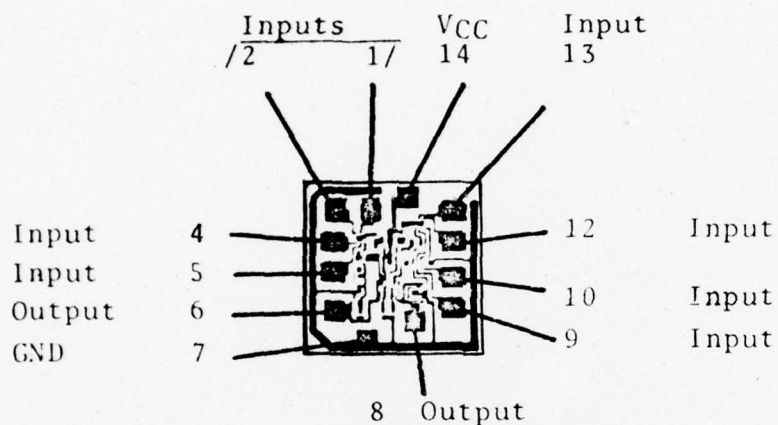
Typical Diode Configurations
(Dimensions shown are mils.)



No examples of beam-leaded semiconductors are depicted. At this time, the availability of beam-leaded dice is not good. They are difficult to produce, only limited types are being made, and manufacturers are quoting long delivery schedules.

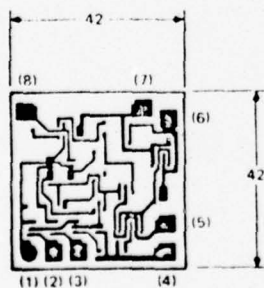
5.3 (Cont.) SEMICONDUCTORS

Examples of Integrated Circuit Configurations



SN54S/74S20

Die Size : 35 x 35



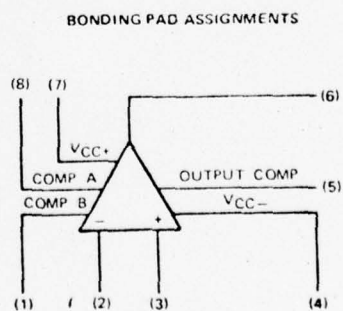
CHIP THICKNESS:
85 ± 1.0

BONDING PADS:
4 x 4 MINIMUM

ALL DIMENSIONS
ARE IN MILS

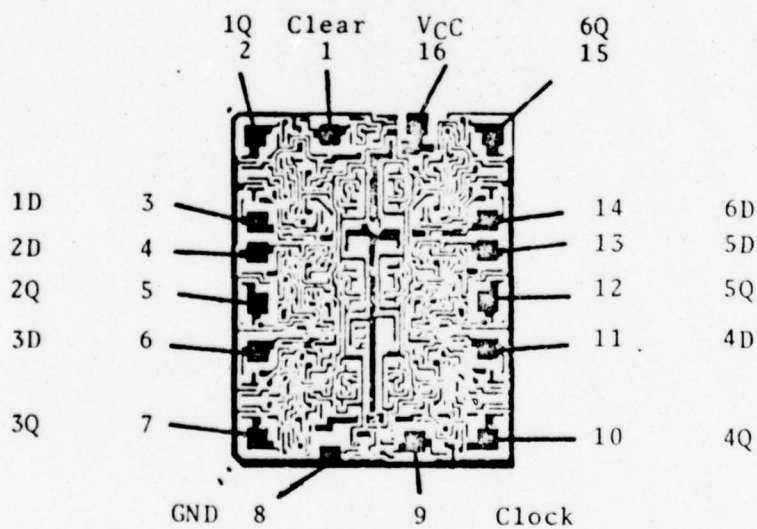
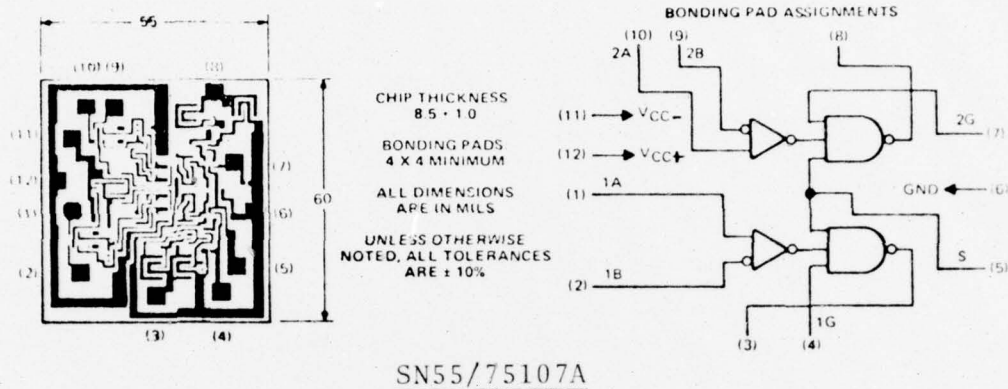
UNLESS OTHERWISE
NOTED, ALL TOLERANCES
ARE ± 10%

LM709/709C



5.3 (Cont.) SEMICONDUCTORS

Examples of Integrated Circuit Configurations

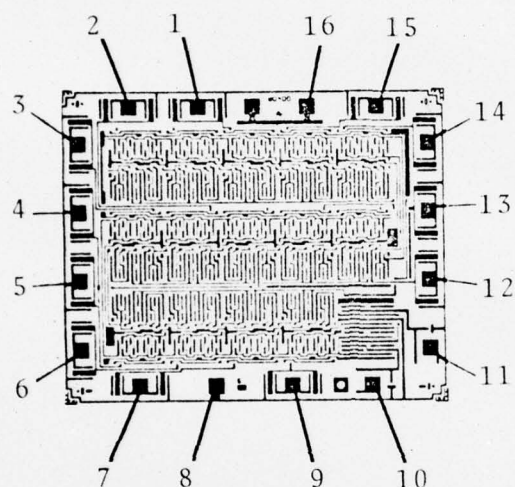


SN54/74174

Die Size : 60 x 75

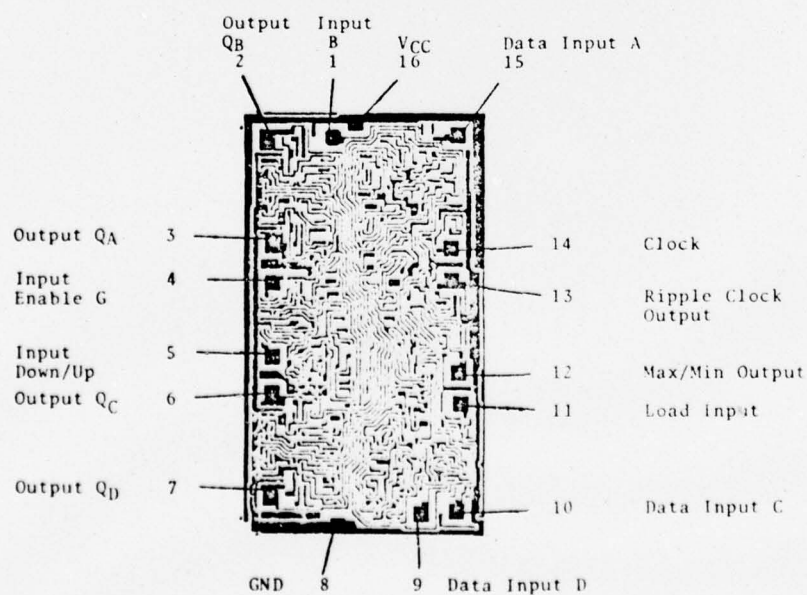
5.3 (Cont.) SEMICONDUCTORS

Examples of Integrated Circuit Configurations



4040A CMOS

Die Size: 110 x 91



SN54/74190

Die Size : 71 x 120

5.3 (Cont.) SEMICONDUCTORS

Example of Vendor's Catalog of Available Chips

SECTION I

DIODES

Device Type	Figure	Pg
1N645	1	1-6
1N646	1	1-6
1N647	1	1-6
1N746	4	1-7
1N747	4	1-7
1N748	4	1-7
1N749	4	1-7
1N750	4	1-7
1N751	4	1-7
1N752	4	1-7
1N753	4	1-7
1N754	4	1-7
1N755	4	1-7
1N756	4	1-7
1N757	4	1-7
1N758	4	1-7
1N759	4	1-7
1N914	2	1-6
1N916	2	1-6
1N917	2	1-6
1N957	4	1-7
1N958	4	1-7
1N959	4	1-7
1N960	4	1-7
1N961	4	1-7
1N962	4	1-7
1N963	4	1-7
1N964	4	1-7
1N965	4	1-7
1N966	4	1-7
1N967	4	1-7
1N968	4	1-7
1N969	4	1-7
1N970	4	1-7
1N971	4	1-7
1N972	4	1-7
1N973	4	1-7
1N974	4	1-7
1N975	4	1-7
1N976	4	1-7
1N1063	2	1-6
1N1064	2	1-6
1N1600	2	1-6
1N3604	2	1-6
1N3605	2	1-6
1N3606	2	1-6
1N3611	3	1-6
1N3612	3	1-6
1N4001	3	1-6
1N4002	3	1-6
1N4003	3	1-6
1N4004	3	1-6
1N4009	2	1-6
1N4148	2	1-6
1N4149	2	1-6
1N4150	2	1-6
1N4151	2	1-6
1N4152	2	1-6
1N4153	2	1-6
1N4154	2	1-6
1N4245	3	1-6
1N4246	3	1-7
1N4305	2	1-6
1N4370	4	1-7
1N4371	4	1-7
1N4372	4	1-7
1N4444	2	1-6
1N4446	2	1-6
1N4447	2	1-6
1N4448	2	1-6
1N4449	2	1-6

1N4454	2	1-6
1N4531	2	1-6
1N4532	2	1-6
1N4533	2	1-6
1N4536	2	1-6
1N5226	4	1-7
1N5227	4	1-7
1N5228	4	1-7
1N5229	4	1-7
1N5230	4	1-7
1N5231	4	1-7
1N5232	4	1-7
1N5233	4	1-7
1N5234	4	1-7
1N5235	4	1-7
1N5236	4	1-7
1N5237	4	1-7
1N5238	4	1-7
1N5239	4	1-7
1N5240	4	1-7
1N5241	4	1-7
1N5242	4	1-7
1N5243	4	1-7
1N5244	4	1-7
1N5245	4	1-7
1N5246	4	1-7
1N5247	4	1-7
1N5248	4	1-7
1N5249	4	1-7
1N5250	4	1-7
1N5251	4	1-7
1N5252	4	1-7
1N5253	4	1-7
1N5254	4	1-7
1N5255	4	1-7
1N5256	4	1-7
1N5257	4	1-7
1N5258	4	1-7
1N5259	4	1-7
1N5260	4	1-7

TRANSISTORS —

Bi Polar

Device	Figure	Pg
2N697	8	1-8
2N699	8	1-8
2N718	8	1-8
2N718A	8	1-8
2N720	8	1-8
2N720A	8	1-8
2N731	8	1-8
2N870	8	1-8
2N871	6	1-7
2N918	5	1-7
2N930	26	1-14
2N956	6	1-7
2N1613	8	1-8
2N1711	6	1-7
2N1889	8	1-8
2N1890	6	1-7
2N1893	6	1-7
2N2102	6	1-7
2N2192	6	1-7
2N2192A	6	1-7
2N2193	6	1-7
2N2193A	6	1-7
2N2218	7	1-8
2N2219	7	1-8
2N2219A	7	1-8
2N2222	7	1-8
2N2222A	7	1-8
2N2243	8	1-8
2N2243A	8	1-8
2N2369	9	1-8

2N2369A	9	1-8
2N2432	10	1-9
2N2432A	10	1-9
2N2444	26	1-14
2N2605	12	1-9
2N2605	12	1-9
2N2605A	12	1-9
2N2857	Consult Factory	
2N2894	13	1-10
2N2904	14	1-10
2N2905	14	1-10
2N2905A	14	1-10
2N2906	14	1-10
2N2907	14	1-10
2N2907A	14	1-10
2N2944A	15	1-10
2N2945A	15	1-10
2N2946A	15	1-10
2N3011	9	1-8
2N3013	16	1-11
2N3014	16	1-11
2N3015	7	1-8
2N3019	8	1-8
2N3250	18	1-11
2N3250A	18	1-11
2N3251	18	1-11
2N3251A	18	1-11
2N3467	Consult Factory	
2N3468	Consult Factory	
2N3564	5	1-7
2N3565	26	1-14
2N3570	17	1-11
2N3571	17	1-11
2N3572	17	1-11
2N3638	14	1-10
2N3646	13	1-10
2N3702	14	1-10
2N3703	14	1-10
2N3704	7	1-8
2N3705	7	1-8
2N3706	7	1-8
2N3707	26	1-14
2N3708	26	1-14
2N3709	26	1-14
2N3710	26	1-14
2N3711	26	1-14
2N3724	19	1-12
2N3724A	19	1-12
2N3725	19	1-12
2N3725A	19	1-12
2N3829	18	1-11
2N3903	21	1-12
2N3904	21	1-12
2N3905	22	1-13
2N3906	22	1-13
2N4026	Consult Factory	
2N4027	Consult Factory	
2N4028	Consult Factory	
2N4029	Consult Factory	
2N4030	Consult Factory	
2N4031A	Consult Factory	
2N4032	Consult Factory	
2N4033	Consult Factory	
2N4044	Consult Factory	
2N4058	12	1-9
2N4059	12	1-9
2N4060	12	1-9
2N4061	12	1-9
2N4062	12	1-9
2N4138	10	1-9
2N4252	17	1-11
2N4253	17	1-11
2N4260	Consult Factory	
2N4261	Consult Factory	
2N4957	Consult Factory	

5.3 (Cont.) SEMICONDUCTORS

Example of Vendor's Catalog of Available Chips

2N4958	Consult Factory	54/7402	2-18	54/74161	2-41
2N4959	Consult Factory	54/7403	2-19	54/74162	2-41
2N4996	17 1-11	54/7404	2-19	54/74163	2-41
2N4997	17 1-11	54/7405	2-19	54/74164	2-42
2N5058	19 1-12	54/7406	2-20	54/74165	2-42
2N5059	19 1-12	54/7407	2-20	54/74173	2-42
2N5109	Consult Factory	54/7408	2-20	54/74174	2-43
2N5400	14 1-10	54/7409	2-21	54/74175	2-43
2N5401	14 1-10	54/7410	2-21	54/74176	2-43
2N5447	14 1-10	54/7412	2-21	54/74181	2-44
2N5448	14 1-10	54/7413	2-22	54/74182	2-44
2N5449	7 1-8	54/7414	2-22	54/74183	2-44
2N5450	7 1-8	54/7416	2-20	54/74190	2-45
2N5451	7 1-8	54/7417	2-22	54/74191	2-45
2N5550	26 1-14	54/7420	2-23	54/74192C	2-45
2N5551	26 1-14	54/7422	2-23	54/74193C	2-46
		54/7423	2-23	54/74194	2-46
		54/7426	Consult Factory	54/74196B	2-46
		54/7427	2-24	54/74197B	2-47
		54/7428	2-24	54/74368	2-47
		54/7430	2-24		
		54/7432	2-25		
		54/7433	2-25		
		54/7437	2-25		
		54/7438	2-26		
		54/7440	2-26		
		54/7442	2-26		
		54/7443	2-26		
		54/7444	2-26		
		54/7445	2-27		
		54/7446	2-27		
		54/7449	2-27		
		54/7450	2-28		
		54/7451	2-28		
		54/7453	2-28		
		54/7454	2-28		
		54/7460	2-28		
		54/7470	2-29		
		54/7472	2-29		
		54/7473	2-29		
		54/7474	2-30		
		54/7475	2-30		
		54/7476	2-29		
		54/7477	2-30		
		54/7480	2-31		
		54/7482	2-31		
		54/7483A	2-31		
		54/7486	2-32		
		54/7490	2-32		
		54/7491	2-32		
		54/7492	2-33		
		54/7493	2-33		
		54/7494	2-33		
		54/7495	2-34		
		54/7496	2-34		
		54/7497	2-34		
		54/74107	2-35		
		54/74111	2-35		
		54/74116	2-36		
		54/74120	2-36		
		54/74121	2-36		
		54/74122	2-37		
		54/74123	2-37		
		54/74128	2-24		
		54/74136A	2-37		
		54/74141	2-38		
		54/74145	2-15		
		54/74148	2-38		
		54/74151A	2-38		
		54/74153	2-39		
		54/74154	2-39		
		54/74155	2-39		
		54/74156	2-40		
		54/74157	2-40		
		54/74160	2-40		

TRANSISTORS — J-

FETs

Device	Figure	Pg
2N3684	27	1-15
2N3685	27	1-15
2N3686	27	1-15
2N3687	27	1-15
2N3819	20	1-12
2N3821	20	1-12
2N3822	20	1-12
2N3823	20	1-12
2N3824	20	1-12
2N3921	35	1-15
2N3954	33	
2N3955	33	
2N3993A	23	1-13
2N3994	23	1-13
2N4091	29	1-15
2N4092	29	1-15
2N4093	29	1-15
2N4117	32	1-15
2N4118	32	1-15
2N4119	32	1-15
2N4338	27	1-15
2N4339	27	1-15
2N4340	27	1-15
2N4341	27	1-15
2N4391	25	1-14
2N4392	25	1-14
2N4393	25	1-14
2N4416	31	1-15
2N4416A	31	1-15
2N4446	30	1-15
2N4448	30	1-15
2N4856	25	1-14
2N4857	25	1-14
2N4858	25	1-14
2N4859	25	1-14
2N4860	25	1-14
2N4861	25	1-14
2N5018	37	1-16
2N5019	37	1-16
2N5114	37	1-16
2N5115	37	1-16
2N5116	37	1-16
2N5163	28	1-15
2N5248	20	1-12
2N5432	30	1-15
2N5433	30	1-15
2N5434	30	1-15

SECTION 2

STD TTL

Device Type	Pg
54/7400	2-18

SECTION 3

SCHOTTKY TTL

Device Type	Pg
54/74S00	3-49
54/74S02	3-49
54/74S03	3-49
54/74S04	3-50
54/74S10	3-50
54/74S11	3-50
54/74S20	3-51
54/74S22	3-51
54/74S40	3-51
54/74S51	3-49
54/74S64	3-52
54/74S74	3-52
54/74S112	3-52
54/74S113	3-53
54/74S135	3-53
54/74S138	3-53
54/74S139	3-54
54/74S140	3-51
54/74S151	3-54
54/74S153	3-54
54/74S157	3-55
54/74S174	3-55
54/74S175	3-55
54/74S181	3-56
54/74S182	3-56
54/74S194	3-56
54/74S195	3-57
54/74S251	3-57
54/74S257	3-57
54/74S258	3-58
54/74S280	3-58

SECTION 4

LOW POWER TTL

Device Type	Pg
54/74L00	4-60
54/74L02	4-60
54/74L04	4-60
54/74L10	4-60
54/74L20	4-61
54/74L30	4-61
54/74L42	4-61
54/74L51	4-61
54/74L54	4-62
54/74L55	4-62
54/74L71	4-62
54/74L72	4-62
54/74L73	4-6
54/74L74	4-63

5.3 (Cont.) SEMICONDUCTORS

Example of Vendor's Catalog of Available Chips

54/74L75	4-63	54LS/74LS125	5-82	LM747	6-103
54/74L85	4-83	54LS/74LS126	5-82	NE/SE536	6-103
54/74L86	4-64	54LS/74LS132	5-83	NE/SE555	6-104
54/74L90	4-64	54LS/74LS136	5-83	uA740	6-103
54/74L91	4-64	54LS/74LS138	5-83	MC1456/1536	6-103
54/74L93	4-64	54LS/74LS139	5-83	MC1458/1558	6-104
54/74L95	4-65	54LS/74LS145	5-84	MC1496/1596	6-104
54/74L121	4-65	54LS/74LS151	5-84	55/75107A	6-105
54/74L122	4-65	54LS/74LS153	5-84	55/75108A	6-105
54/74L123	4-65	54LS/74LS155	5-84	55/75109A	6-105
54/74L153	4-66	54LS/74LS156	5-85	55/75110A	6-106
54/74L154	4-66	54LS/74LS157	5-85	55/75112	6-106
54/74L157	4-66	54LS/74LS158	5-85	55/75113	6-106
54/74L164	4-66	54LS/74LS160	5-85	55/75115	6-107
54/74L192	4-67	54LS/74LS161	5-86	55/75138	6-107
54/74L193	4-67	54LS/74LS162	5-86	55/75188	6-107

SECTION 5 LOW POWER SCHOTTKY TTL

Device Type	Pg	54LS/74LS174	5-87	55/75363	6-110
54LS/74LS00	5-69	54LS/74LS175	5-88	55/75450B	6-111
54LS/74LS01	5-69	54LS/74LS181	5-88	55/75451B	6-111
54LS/74LS02	5-69	54LS/74LS190	5-88	55/75452B	6-112
54LS/74LS03	5-69	54LS/74LS191	5-88	55/75453B	6-112
54LS/74LS04	5-70	54LS/74LS192	5-89	55/75454B	6-113
54LS/74LS05	5-70	54LS/74LS193	5-89	55/75461	6-113
54LS/74LS08	5-70	54LS/74LS194	5-89	55/75463	6-114
54LS/74LS09	5-70	54LS/74LS195	5-89	55/75462	6-114
54LS/74LS10	5-71	54LS/74LS196	5-90	55/75464	6/115
54LS/74LS11	5-71	54LS/74LS197	5-90	55/75480	6-115
54LS/74LS12	5-71	54LS/74LS221	5-90	55/75481	6-116
54LS/74LS13	5-71	54LS/74LS247	5-90	55/75486	6-116
54LS/74LS14	5-72	54LS/74LS248	5-91	55/75487	6-117
54LS/74LS15	5-72	54LS/74LS249	5-91		
54LS/74LS20	5-72	54LS/74LS251	5-91		
54LS/74LS21	5-72	54LS/74LS253	5-91		
54LS/74LS22	5-73	54LS/74LS257	5-92		
54LS/74LS27	5-73	54LS/74LS258	5-92		
54LS/74LS28	5-73	54LS/74LS259	5-92		
54LS/74LS30	5-73	54LS/74LS261	5-92		
54LS/74LS32	5-74	54LS/74LS266	5-93		
54LS/74LS33	5-74	54LS/74LS279	5-93		
54LS/74LS37	5-74	54LS/74LS283	5-93		
54LS/74LS38	5-74	54LS/74LS290	5-93		
54LS/74LS40	5-75	54LS/74LS293	5-94		
54LS/74LS42	5-75	54LS/74LS295A	5-94		
54LS/74LS47	5-75	54LS/74LS298	5-94		
54LS/74LS48	5-75	54LS/74LS365	5-94		
54LS/74LS49	5-76	54LS/74LS367	5-95		
54LS/74LS51	5-76	54LS/74LS368	5-95		
54LS/74LS54	5-76	54LS/74LS386	5-95		
54LS/74LS55	5-76	54LS/74LS395	5-95		
		54LS/74LS670	5-95		

SECTION 7

CMOS

Device Type	Pg
4001A	7-119
4002A	7-119
4007A	7-119
4008A	7-119
4009A	7-120
4010A	7-120
4011A	7-120
4011B	7-120
4012A	7-121
4013A	7-121
4013B	7-121
4014A	7-121
4015A	7-122
4016A	7-122

SECTION 7

CMOS

Device Type	Pg
4001A	7-119
4002A	7-119
4007A	7-119
4008A	7-119
4009A	7-120
4010A	7-120
4011A	7-120
4011B	7-120
4012A	7-121
4013A	7-121
4013B	7-121
4014A	7-121
4015A	7-122
4016A	7-122
4017A	7-122
4018A	7-122
4019A	7-123
4020A	7-123
4021A	7-123
4022A	7-123
4023A	7-124
4024A	7-124
4025A	7-124
4027A	7-124
4028A	7-125
4029A	7-125
4030A	7-125
4040A	7-125
4042A	7-126
4043A	7-126
4044A	7-126
4049A	7-126
4050A	7-127
4051A	7-127
4052A	7-127
4053A	7-127

SECTION 6

LINEARS

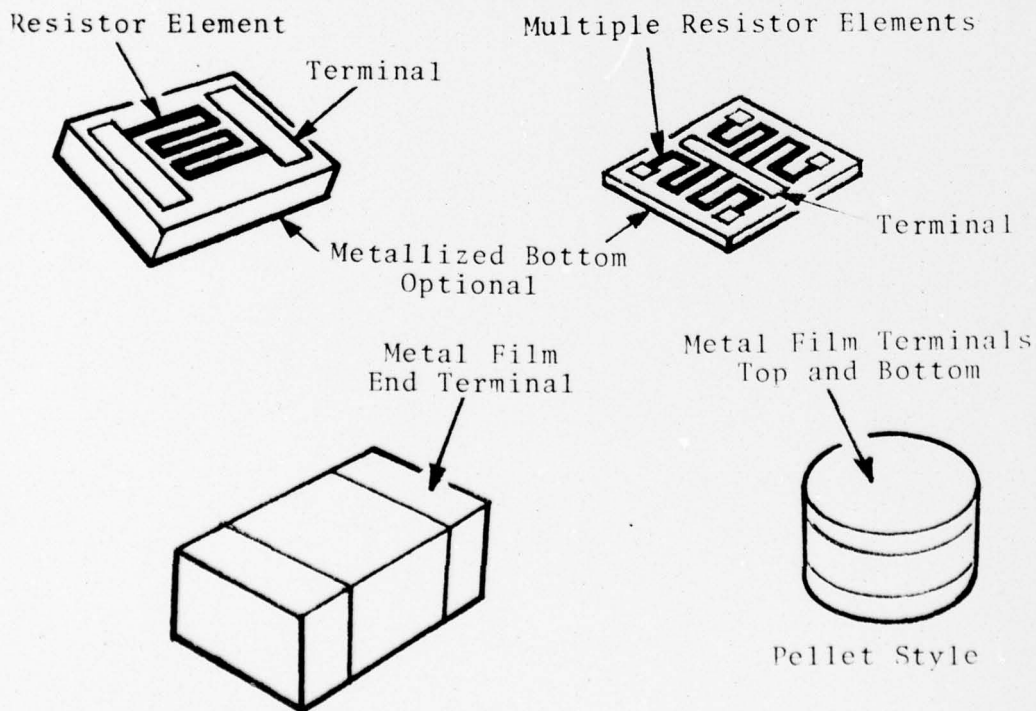
Device Type	Pg
LM101	6-97
LM104	6-97
LM105	6-98
LM106	6-98
LM107	6-98
LM108	6-99
LM109	6-99
LM111	6-99
LM119	6-100
LM124	6-100
LM139	6-100
LM709	6-101
LM710	6-101
LM711	6-101
LM723	6-102
LM733	6-102
LM741	6-102

5.4 RESISTORS

Hybrid resistors, besides being fabricated integral to the substrate, can be installed as components. As components, they can be pretested before mounting on the substrate. Sizes, values, and tolerances vary over wide ranges to suit almost any circuit requirement.

Component resistors intended for hybrid use are available in many types. Some commonly used types are thick or thin films on the surface of ceramic chips, silicon chips with diffused resistors on the top surfaces, ceramic chips with end terminals, pellet types with terminals top and bottom. Terminals can be various metals with various platings.

Examples of Component Resistors



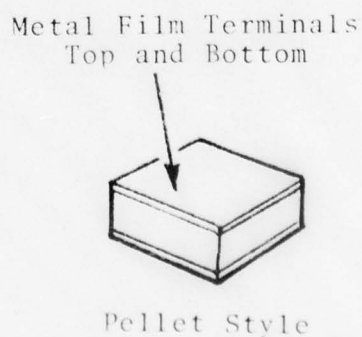
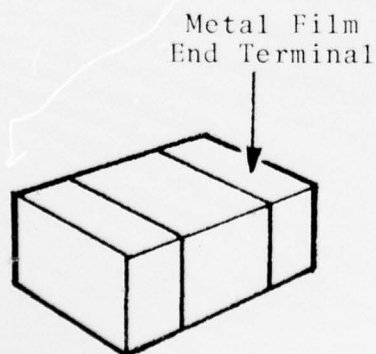
5.5 CAPACITORS

Capacitors suitable for use in hybrids are available in a wide range of values, sizes, and voltage ratings. High Q capacitors are available for microwave applications.

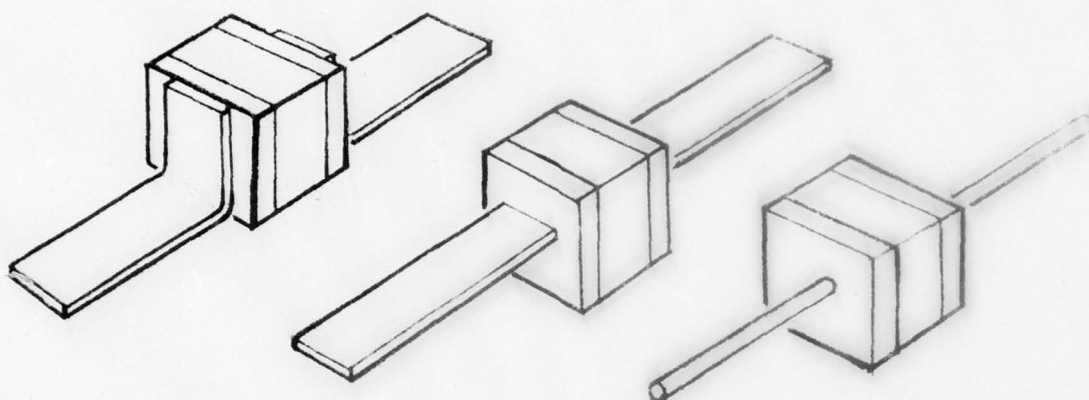
Pellet style capacitors are available in sizes as small as .020 x .020 x .010 in. high (.508 x .508 x .254 mm). Ceramic chip capacitors with end terminals are as small as .050 x .050 x .040 in. high (1.27 x 1.27 x 1.016 mm).

Capacitors can have metal film terminals of various metals. Commonly used materials are silver, palladium silver, gold. Capacitors can have wire or ribbon leads of various materials. Tinned copper, gold plated nickel, silver are frequently used.

Variable capacitors are available in sizes suitable for hybrids. However, if sealed inside a package, then subjected to various stresses (especially vibration) the value might change and the adjustment would be inaccessible.

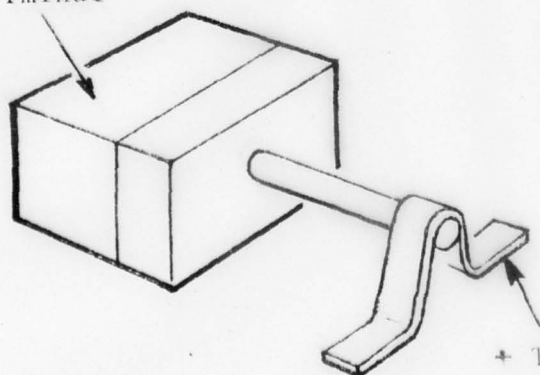


5.5 (Cont.) CAPACITORS

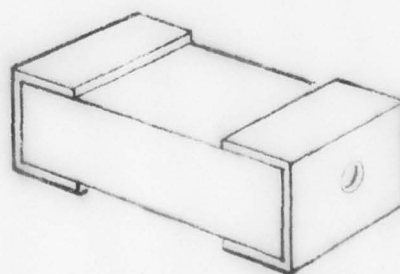


Tantalum Capacitors

Metal Film
Terminal



+ Terminal



5.6 SOLDERS

Solders used in hybrids are available in various compositions and in various forms. Pastes, sheets, performs, wires, or pellets are all available having a range of melting temperatures.

Thin sheets of film solder are available from which any shape can be cut. Preforms, die cut from sheets, are available in rectangular shapes for die-attach or picture frames for cover sealing (just to name a few). Paste solders can be screen printed on substrates and later reflowed to attach components. The conductor tracks on a substrate are sometimes plated or dipped to create a solder coat prior to installing components.

Since temperature stepping is often a consideration in hybrid assembly and rework, a variety of solders is often used in one hybrid. Solders containing varying amounts of indium are often used for their low temperature and/or low leaching characteristics.

Examples of commonly used solders and their melting temperatures are shown below.

Solder Compositions (%)			Melting Temp.	Typical Applications
97	Gold	3 Silicon	370°C	Die Attach
80	Gold	20 Tin	280°C	Cover Seal Component-Attach Substrate Installation
63	Tin	37 Lead	183°C	Cover Seal
60	Tin	40 Lead	188°C	Component Attach Substrate Installation
79	Indium	15 Lead	149°C	Substrate Installation
5	Silver			Component Attach Rework

5.7 EPOXIES

Many types of epoxies are available from which the choice can be made to best suit the application. Electrically conductive and non-conductive properties are available as well as air drying or heat curing. Epoxies can be single composition or may require adding a hardener. Some require refrigerated storage. The choice usually depends on the epoxy's suitability for manufacturing processes, its electrical properties over long periods of time and under various environmental stresses, and its bond integrity. Since only small, low-weight parts are being bonded with the epoxy, high bond strength is typically not as important as the integrity of the bond over time and environmental stresses.

Epoxy used for component attachment, because it is inside a sealed package, may not need to emphasize moisture resistance; whereas, one used for cover sealing might need to resist moisture. All epoxies used in hybrids need to withstand the temperatures of environmental testing and the continuous operating temperature of the hybrid's final application without degrading their properties.

Conductive epoxies usually contain certain powdered metal to provide the conductivity characteristic.

Some epoxies are advertised to have no significant outgassing at temperatures up to 190°C and under a vacuum of 10^{-8} torr.

Epoxies can also be obtained as die cut preforms. One commonly used shape is a picture frame type suitable for cover sealing.

5.7 (Cont.) EPOXIES

Some examples of epoxy properties are as follows:

Volume Resistivity (conductive); .0001 Ω cm
(for a 50 mil (1.27 mm) square die-attach, this
is $1.6 \times 10^{-5} \Omega$)

Silver epoxy advertised as having .0001 Ω cm
volume resistivity at temperatures up to 400°C,
and the same resistivity after 1,000 hours at
150°C.

Volume Resistivity (non-conductive); $2 \times 10^{15} \Omega$ cm.

Useable Temperature; 250°C continuously, 350°C
for short time.

5.8 INTERCONNECTING WIRES

Although 1 mil (0.0254 mm) diameter is the size most commonly
used for aluminum and gold wire bonding, the other available
sizes are 0.7 mil (0.0178 mm), 1.5 mils (0.0381 mm), and 2
(0.0508 mm) through 10 mils (0.254 mm) in 1-mil increments.

The aluminum wire composition is typically 99% aluminum with
1% silicon. The tensile strength of the 1 mil size is 14 to
18 grams. The resistance of 100 mils (2.54 mm) of length
is approximately 0.023 Ω .

The gold wire is typically 99.9% pure. The tensile strength
of the 1 mil size is 5 to 9 grams. The resistance of 100 mils
(2.54 mm) of length is approximately 0.018 Ω .

SECTION 6 FABRICATION AND ASSEMBLY PROCESSES

The processes, techniques and equipment described in this section are those generally used in the fabrication and assembly of hybrid microcircuits. What is being achieved by each process step is more significant than how it is being achieved, because there are many differences between individual manufacturing groups and especially because the technology is constantly improving.

6.1 THIN FILM SUBSTRATE FABRICATION

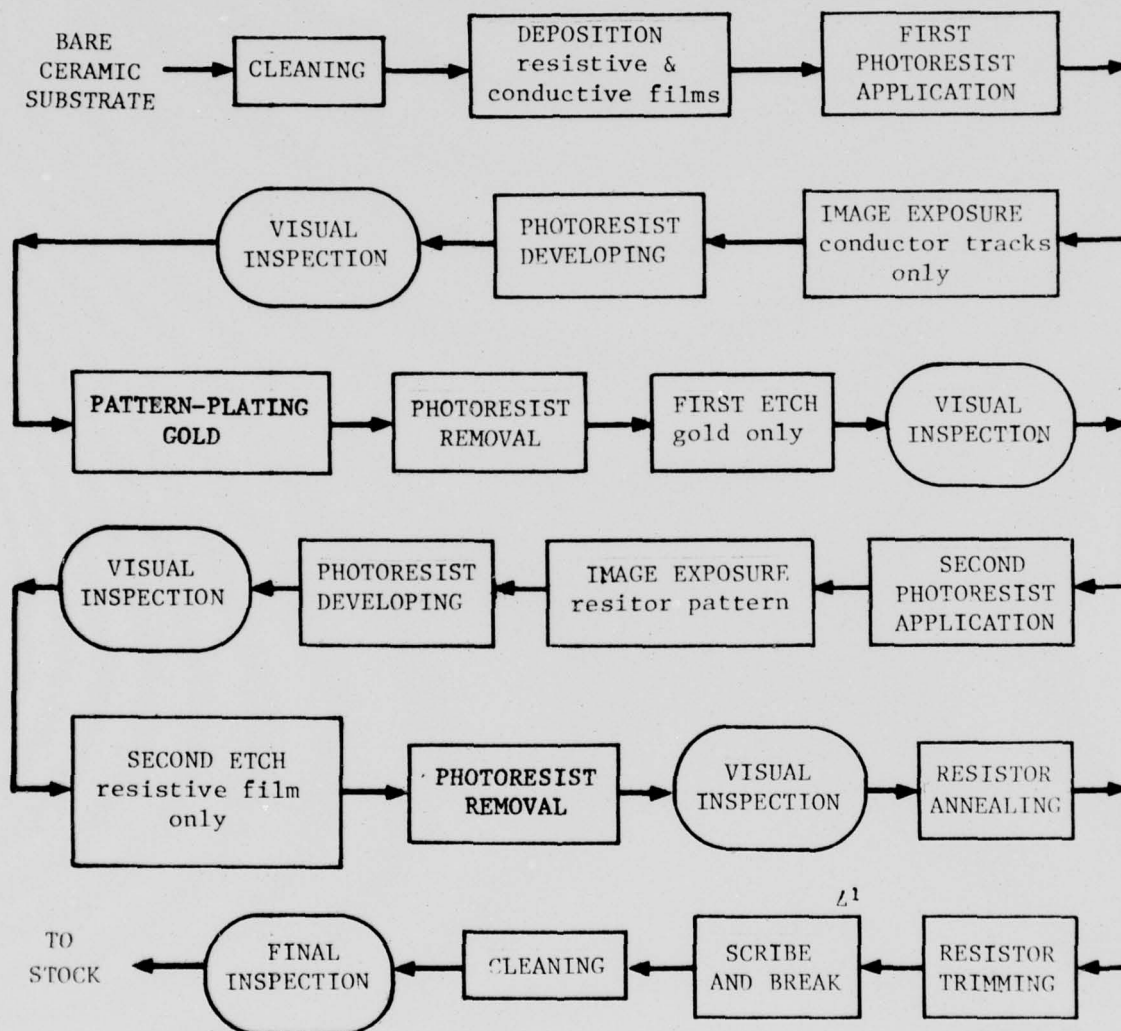
The sequence of fabrication processes for thin film substrates is shown in Figures 6.1-1 and 6.1-2. This text describes the processes called out in these figures. (Also see Section 8.1.)

Substrate Cleaning. The first requirement in the fabrication cycle is to assure the cleanliness of the substrate surface. Foreign matter on the surface will prevent the adherence of material deposited on that surface. Many different materials and techniques are used for cleaning. One important requirement is that the cleaning process insure that there is no residue of the cleaning materials themselves.

Vacuum Deposition. The cleaned substrates are placed in a deposition chamber in order to apply the resistive and conductive films. The deposition equipment is either a thermal evaporator or a sputtering chamber.

A thermal evaporator is commonly a bell jar. The resistive and conductive materials, in bulk form, are placed in a crucible in the center of the bell jar base. The substrates are placed around and above the crucibles, in some form of holding frame,

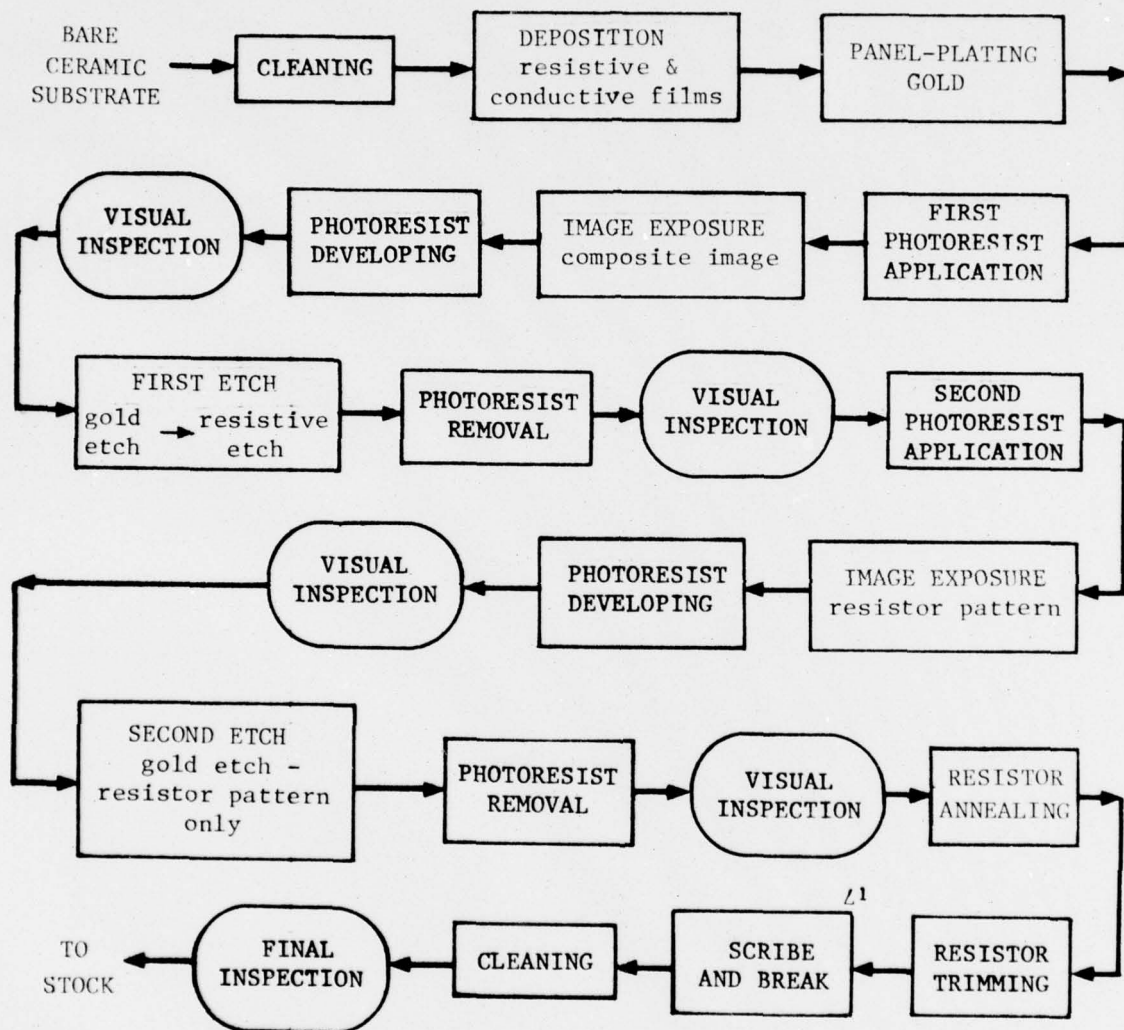
6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION



^{L1} This process required if ceramic contains multiple images of a smaller sized substrate, or if an individual image was fabricated on an oversized ceramic.

Figure 6.1-1 SEQUENCE OF THIN FILM SUBSTRATE FABRICATION PROCESS USING PATTERN-PLATING TECHNIQUES

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION



^{L1} This process required if ceramic contains multiple images of a smaller sized substrate, or if an individual image was fabricated on an oversized ceramic.

Figure 6.1-2 SEQUENCE OF THIN FILM SUBSTRATE FABRICATION PROCESSES USING PANEL-PLATING TECHNIQUES

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

so that the substrate surfaces are approximately perpendicular to the center of the crucible. The bell jar is placed in position over the substrates and crucibles, and a vacuum is created inside the jar. The resistive material is deposited first. The material is raised to vaporization temperature, at which time molecules of the bulk material evaporate out of the crucible. From the crucible, the molecules move in an approximately straight path in all directions and deposit themselves on whichever surface they contact. The entire inside surface of the bell jar, as well as the substrates, becomes coated.

A sputtering chamber operates on a different principal than a thermal evaporator. The substrates are laid flat on a circular tray, which is placed flat on the base of the vacuum chamber. The bulk materials, preformed into disk shapes (called targets), are held in place by a frame inside the chamber so that one flat surface of the target is parallel to the substrate surfaces.

The chamber is sealed and a vacuum is created inside. A small quantity of argon gas is introduced into the vacuum. The gas is made to ionize. The target is electrically polarized to a positive charge (opposite polarity from the ionized gas). The ions are attracted, at a high velocity, to the opposite polarity of the target. The ions impact the surface of the target, knocking molecules off the target. These molecules migrate and deposit themselves on any surface they contact.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

The most widely used resistive material is nickel chromium (commonly called nichrome). The resistivity of nichrome typically will be within the range from 25 to 250 ohms per square (Ω / \square). The thickness will typically be within the range from 100 to 750 \AA .

Tantalum nitride is another resistive material frequently used. Its resistivity is typically within the range from 100 to 600 Ω / \square .

Cermet is used occasionally. Its resistivity is typically within the range from 300 to 1,000 Ω / \square .

The circular tray revolves like a carousel, bringing each substrate into the path of the molecules being "sputtered" off the target.

The gold conductive film is deposited after the resistive film, and is deposited by a repeat of the previous process, without opening the sealed chamber. The gold is not applied to the full thickness required for the substrate electrical function. Only sufficient gold ($\approx 1500 \text{\AA}$) is applied to make the substrate surface conductive enough for subsequent electroplating processes.

Several factors are related to the ultimate resistivity attained in a sputtering run. Among these are:

- 1) the integrity of the vacuum prior to introduction of argon
- 2) the amount of argon introduced

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

- 3) the relative power required to cause ionization and target bombardment
- 4) the length of time that substrates are exposed to the target being bombarded

All of these affect the final thickness of the sputtered film and, therefore, the resistivity of that film.

The seal is then broken on the vacuum chamber; the chamber is opened, and the substrates are removed.

The important criteria for the deposition process are control of the thickness of the deposited films and uniformity of the coating (i.e., no pin holes). The sheet resistivity (rated in ohms per square) of the resistive film is determined mainly by the film thickness.

Panel-Plating Gold. Only in the panel-plating method is the gold plating done after deposition. In the pattern-plating method, gold plating is done after the photoresist has been exposed and developed. In the panel-plating method, the entire surface of the deposited gold film is plated to increase the thickness to the final dimension (typically 50 μ in. (1.27 μ m) or greater. The thickness and porosity of the plating are determined by the amperage of the plating current compared to the area being plated (this ratio is called "current density"), the concentration of the plating solution, and the length of plating time. The technique derives its name from this process step. The criteria for panel-plating gold are: control of the current density, control of the plating solution, and control of the plating time.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

First Photoresist Application. A photosensitive material (called photoresist) is next applied over the surface of the gold. (For panel-plating, this is plated gold. In pattern-plating, this is the deposited gold.) The bulk photoresist can be applied as a dry film sheet or as a liquid. The photoresist can be either negative or positive type.

Dry film resist is typically thicker than liquid resist. The dry is used to achieve a uniform thickness over a larger area, or when subsequent gold plating will be done to a thickness greater than 200 μ in.

The photosensitive dry film is prelaminated on a thin, clear plastic sheet, and the resulting composite is typically supplied in a roll. Prior to applying the dry film to the substrate surface, both the substrate and dry film are warmed to approximately 90°C. While still warm, the substrate is pressed to the film. The dry film, along with its clear plastic cover, adheres to the substrate. (The clear plastic will be removed after exposure.) After cooling, the dry film is ready for exposure through the clear plastic.

Liquid resist can be applied to the substrate in several ways. The substrate can be dipped into a container of liquid resist. The substrate can be passed under a roller that is coated with resist (similar to the ink rollers in a printing press). Another method is to flood the substrate with resist, then spin the substrate. Spinning causes the resist to spread evenly over the surface and the excess resist to be flung off the substrate edges. The resist can also be applied through a spray gun.

After application, the liquid resist is air-dried, then oven-baked.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

The criteria for photoresist application are: uniform resist thickness, complete surface coverage, and good adherence to the substrate surface.

Image Exposure. After photoresist application, the 1x scale conductor mask is used to expose the photoresist. The mask may be either glass or film. Glass masks can have their patterns in emulsion or in metal. If the substrate has excessive camber (curvature) a film mask can conform to the curvature. Glass cannot. Mask alignment equipment can be used if the images are very small, or if the alignment of the image is critical. Manual manipulation of the mask by the operator while viewing through a standard microscope is sufficient in most cases. When the mask is properly aligned, a low vacuum is often used to hold the mask in position. When certain alignment equipment is used, the mask does not contact the resist. The light rays are very well collimated, thus eliminating the need for contact.

Ultraviolet light is then exposed onto the photoresist through the clear areas of the mask. If the photoresist is a negative type, the light causes it to polymerize. Positive resist experiences a molecular breakdown where the light strikes. The light is maintained for a specified time. This timing is important to create a good image in the resist. The exposure time depends on the sensitivity of the photoresist.

Even when the mask does contact the resist, collimated light is often used to reduce the spreading of the light rays, thus giving better image resolution. After exposure, the vacuum is released and the mask removed from the substrate.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

In the pattern-plating method, the image on the mask is of the conductor tracks only. In the pattern plating method, the image is a composite of both the conductor tracks and the resistors.

The criteria for the exposure process are proper alignment of the image to the substrate, and proper exposure time.

Photoresist Developing. After image exposure, the substrates are immersed into or sprayed with a solution that dissolves only the non-polymerized or soft resist. For panel-plating, only the composite image is now covered by resist. For pattern-plating, only the conductor image is now exposed. The remaining photoresist is next air dried. Sometimes oven baking is done to insure better adhesion.

The criteria for the developing process are control of the solution strength, time of developing, equal distribution of the solution over all areas of the substrate and complete removal of all unwanted resist.

Visual Inspection. After developing, the image should be visually inspected under non-ultraviolet light.

The criteria for inspection are complete development, no overdevelopment, image resolution, no pin holes in the resist, and proper alignment.

Rejects at this point in the sequence can have the photoresist removed and new resist applied. The substrate can then be recycled through Image Exposure and Developing.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

Pattern-Plating Gold. Only in the pattern-plating method is the gold plating done after photoresist developing. In this plating process, gold is plated only in the conductor image areas. (These are the only exposed areas.) The substrate surface now has thick gold in the image area and thin gold everywhere else.

In addition to the criteria described for panel-plating, pattern-plating must have good image resolution (i.e., the plating must completely cover the exposed area but not spread under the photoresist).

Photoresist Removal. For pattern-plating, the resist is removed before etching. For panel-plating, the resist is removed after etching. The removal process consists of subjecting the substrate to a solution (different from the developing solution) that removes the hardened photoresist.

The criterion for photoresist removal is no residue of either resist or removal solution.

First Etching. In the panel-plating method, there are two etching steps involved in this process. First the exposed gold is etched down to the resistive film. The substrate is then transferred to another etching station where the newly exposed resistive film is etched down to the bare ceramic.

After etching, the substrate surface consists of photoresist (in the composite image) over thick gold, with resistive film under the gold. Bare ceramic is exposed everywhere other than the composite image.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

In pattern-plating, the photoresist has already been removed (see Figure 6.1-1). The surface has thick gold in the area of conductor tracks only and thin gold everywhere else.

The entire surface is subjected to a gold-etchant solution (Potassium Iodide, Potassium Cyanide, or Aqua Regia). This etching continues only until the thin gold is completely gone. The surface of the thick gold has also been etched; but because the etching-time stops when the thin gold is gone, the thick areas are simply reduced in thickness by a small percentage.

After etching, the surface of the substrate consists of a complete layer of resistive film covered with thick gold only in the areas of the conductor tracks.

The criteria for the etching process are control of the strength and temperature of the etchant and close control of the etching time. In panel-plating, the gold being etched is thick, so the chances are greater for the etchant to etch under the photoresist.

Visual Inspection. Inspection at this time is concerned with the effects of etching. Complete etching is required, and only a small undercut is acceptable.

Second Photoresist Application. The previous description of photoresist application is applicable at this point in the sequence.

The criteria of uniform coverage and good adhesion are more difficult to maintain, because the surface is no longer flat. The etching process has removed material from certain areas.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

Image Exposure. The previous description is applicable here.

Photoresist Developing. The previous description is applicable but timing is even more important because any overdeveloping can do more harm on an uneven surface.

Visual Inspection. The inspection at this stage must assure good adhesion and image resolution over the raised edges of the previously etched films. Rejects can be recycled.

Second Etch. The second etch is performed by the same process as previously described. The adhesion and resolution of the photoresist as well as the control of the etching-time are the important factors.

In pattern-plating, the exposed resistive film is etched.

In panel-plating, the thick told is etched in the areas of the resistor pattern only.

Photoresist Removal. The previous description is applicable here.

Visual Inspection. The inspection at this point looks for complete etching and minimal undercut.

Resistor Annealing. This process subjects the substrate to 300°C for approximately two hours in order to stabilize the resistor material before trimming.

Resistor Trimming. Before lasers were introduced, the most common method of trimming thin film resistors was to use an electrically charged needle point.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

when the charged point was brought close to the resistor, an electrical arc formed between the two. This arc would burn a small hole through the resistor material exposing the bare ceramic below. By repeated arcing and by manipulating the substrate under the point, a line was cut into the resistor shape. This cutting reduced the effective width of the resistor, and in so doing increased the resistor value. The manipulation of the substrate was controlled by an x-y table. The resistor value was measured while the trimming process was being done; and the process was stopped when the desired value was reached.

Trimming with a charged needle can consistently achieve accuracies of approximately $\pm 5\%$ of the desired value. Manual movement of the substrate was a time consuming process.

Laser trimming accomplishes the cutting of the resistor by focusing the laser beam in a small spot. The intense heat generated in that spot burns away the resistor material. The size of the spot is controlled much better than with electrical arcing. The size of the spot is approximately 0.5 mils (0.0127 mm) diameter. Manual manipulation of the substrate is still widely used. Accuracies of $\pm 0.01\%$ can be achieved.

Automatic, programmable laser trimming equipment is also available. This system does not move the substrate. The laser spot is moved to the desired locations by the manipulation of reflective mirrors.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

When the substrate is properly aligned in the work station, multiple probes contact the end-terminals of all the substrate resistors simultaneously. The equipment is preprogrammed to measure a resistor value, trim the resistor to a higher value if necessary, then move on to the next resistor on the substrate. It repeats this sequence for all the resistors on one substrate without movement of either the substrate or the probes.

Preprogrammed trimming can be done very fast, 50 resistors in 15 seconds is not unusual. Accuracies of $\pm 0.05\%$ of desired values is to be expected in this high speed mode. Repeatable accuracies of $\pm 0.002\%$ are readily achieved in a slower trimming mode, when necessary.

Dynamic trimming can be performed on those resistors whose final value cannot be determined until the resistor is functioning within its electronic circuit. Since dynamic trimming is done to a completely assembled substrate, all handling (especially the placement of the probes) must be done very carefully to avoid damaging components or bonded wires.

The criteria for resistor trimming are accuracy of the final resistor values, no excessive trimming that reduces the resistor size to less than the minimum allowable.

Scribe and Break. This process step is only required if the substrate contains multiple images of a smaller substrate or if an individual image is fabricated on an oversized substrate. It is not unusual that when bare ceramic is not available in the required size then an oversized one is substituted.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION

In this process, a diamond tip is used to scribe lines into the ceramic surface. The scribe lines define the size of the final substrate. The substrate is usually held in a fixed position, and the diamond tip is passed over the substrate surface. The diamond tip must be maintained sharp to ensure sufficient depth of the scribe lines. In addition, the angle of the tip in relation to the substrate surface is critical.

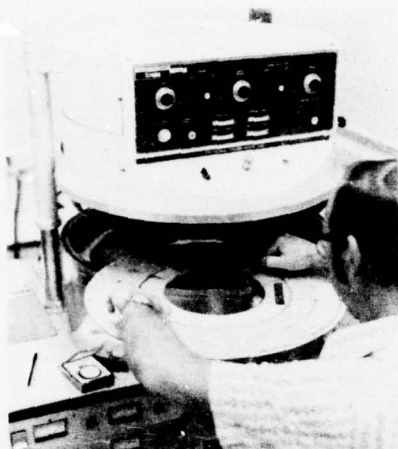
After all scribe lines are created, the substrate is pressed over a straight edge (located along a scribe line) until the substrate breaks along the scribe line. This breaking is repeated at each scribe line. The final result is one or more substrate having the required final size.

The criteria for the scribe-and-break process are accurate location of the scribe lines, and minimum raggedness of the broken edges. The maximum raggedness is dictated by the maximum allowable dimension of the substrate and the proximity of the metallization pattern to the edge of the substrate.

Cleaning. The final cleaning is primarily to remove oils incurred in handling, particles remaining from scribe-and-break and residue or ash from trimming.

Final Inspection. This last inspection is primarily concerned with cleanliness, excessive trimming of the resistors and damage to the substrate pattern due to raggedness of the broken edges.

6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION



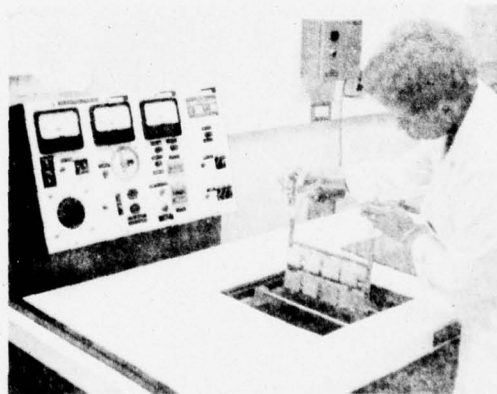
SUBSTRATES ON TRAY BEING
LOADED INTO SPUTTERING CHAMBER



LIQUID PHOTORESIST
ROLLER COATING EQUIPMENT

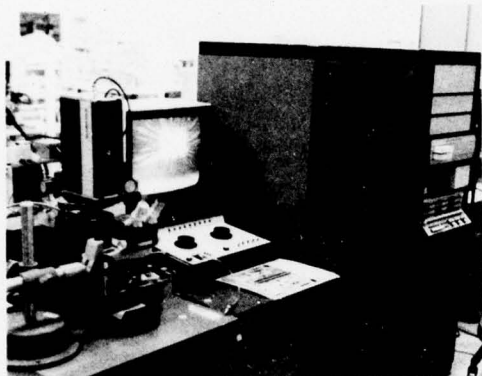


MASK ALIGNMENT EQUIPMENT

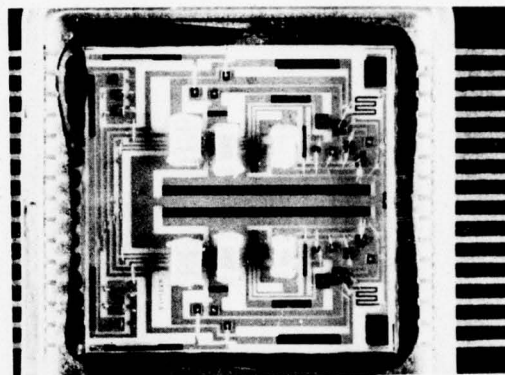


PLATING EQUIPMENT

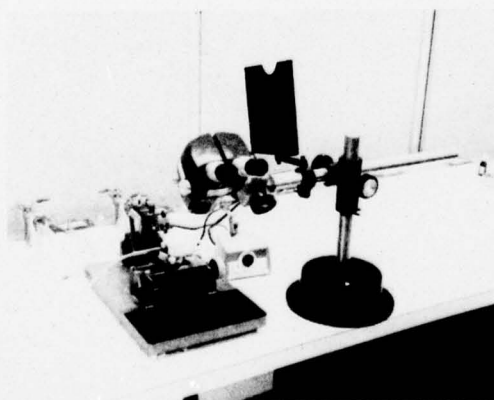
6.1 (Cont.) THIN FILM SUBSTRATE FABRICATION



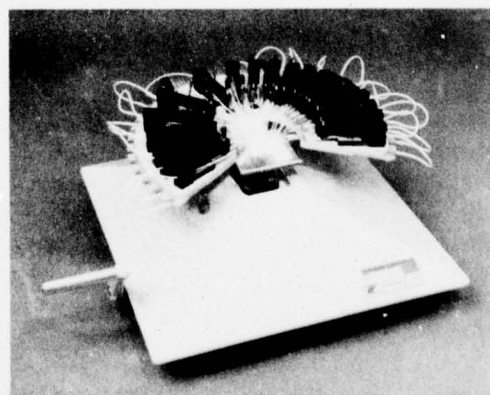
AUTOMATIC PROGRAMMABLE
LASER TRIMMING EQUIPMENT
WITH TELEVISION VIEWING



THIN FILM HYBRID
WITH LASER TRIMMED
RESISTORS



SCRIBE-AND-BREAK EQUIPMENT



MULTIPLE PROBE TEST FIXTURE

6.2 THICK FILM SUBSTRATE FABRICATION

In this section, fabrication processes are described for thick film substrates having a single layer, multiple layers using cross-over dielectric bridges and multiple layers using continuous dielectric planes. The processes described in this text are repeated wherever shown in the flow diagrams. Multilayer substrates require many repeated processes. The double application of the same dielectric pattern is done to prevent pin holes in the dielectric layer.

In thick film fabrication, each image pattern requires a separate screen. The processes used for screen preparation are shown in Figure 6.2-1. (Additional descriptions are in Section 8.2.)

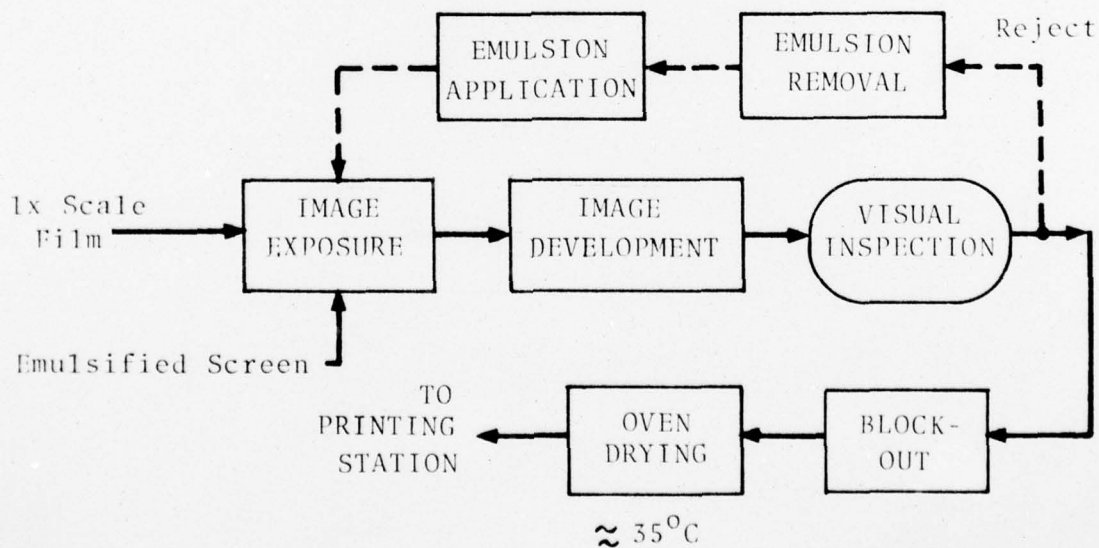
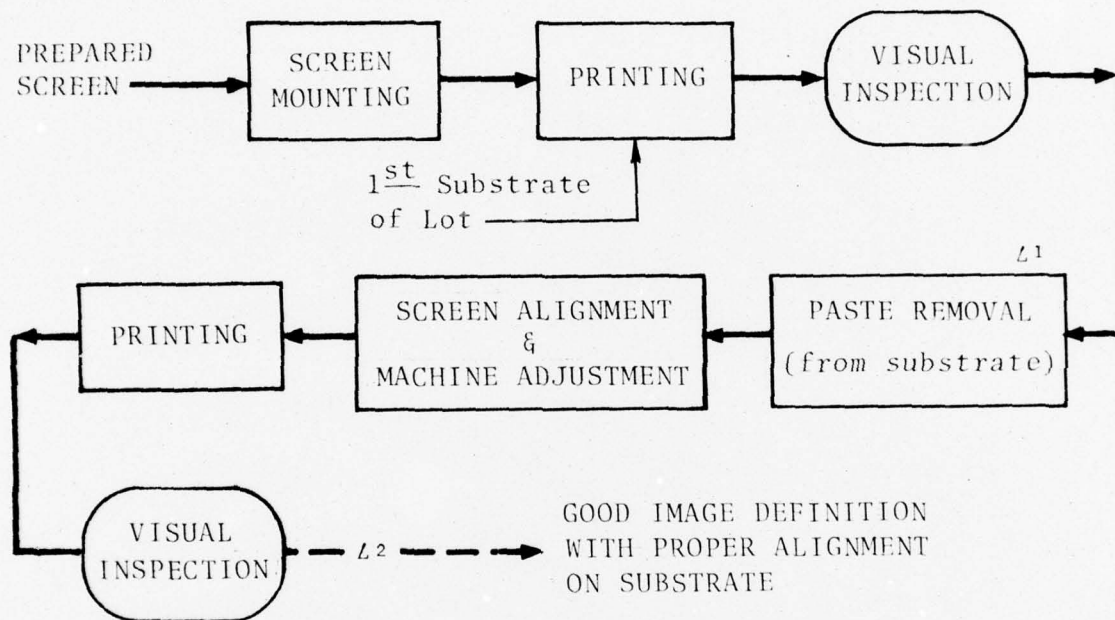


Figure 6.2-1 SEQUENCE OF PROCESSES FOR THICK FILM SCREEN PREPARATION

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION



L1 This operation and all subsequent ones are only required if the image definition or the alignment are not acceptable.

L2 The sequence of Paste Removal, Screen Alignment and Machine Adjustment, Printing, and Visual Inspection is repeated as many times as is necessary.

Figure 6.2-2 PROCEDURE FOR SCREEN INSTALLATION AND MACHINE ADJUSTMENT

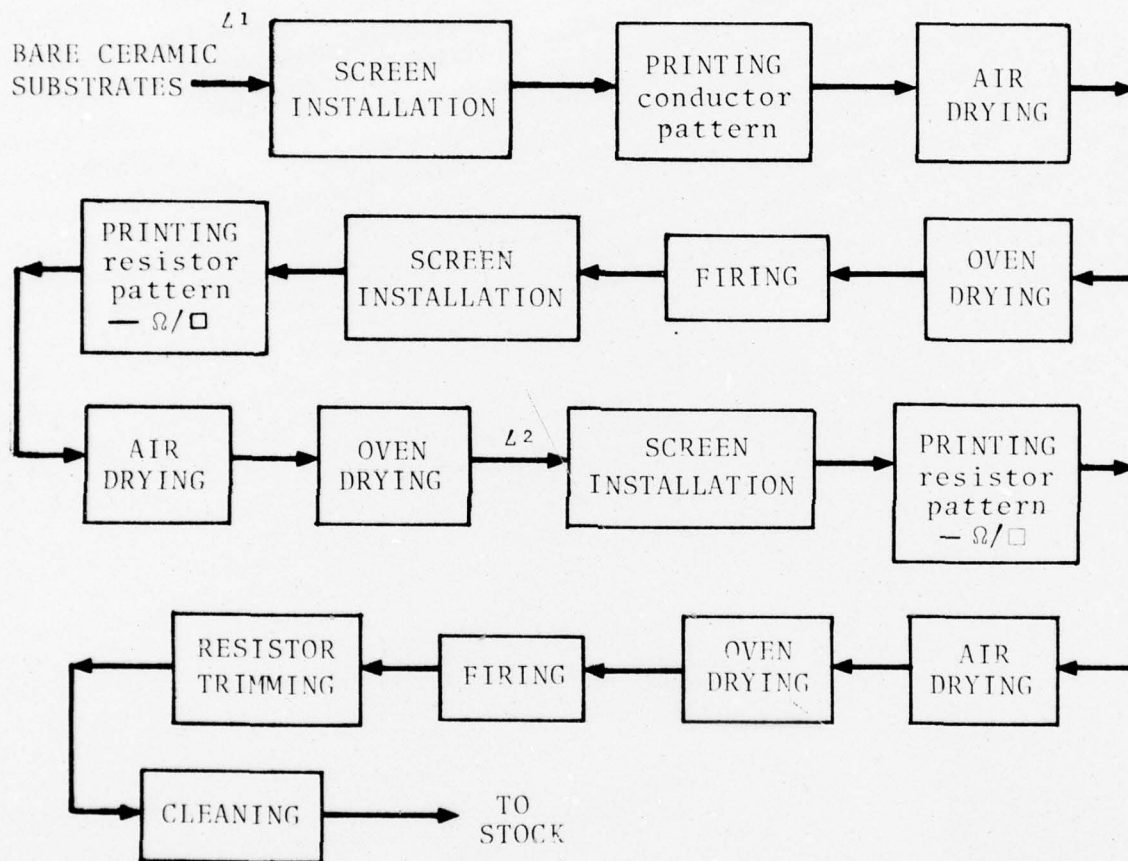
6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Before each new image can be printed on the substrates, the new screen must replace the one previously used in the printer. The new screen must be properly aligned. Screen mounting and alignment consists of the process steps shown in Figure 6.2-2. These several steps are referred to in Figures 6.2-3 through 6.2-5 as "Screen Installation."

The sequence of fabrication processes for single layer substrates is shown in the flow diagram of Figure 6.2-3. The sequence for multilayer substrates using cross-over dielectric bridges is shown in Figure 6.2-4. For multilayer substrates using continuous dielectric layers, the sequence is shown in Figure 6.2-5. Each process step shown in these three flow diagrams is performed on every substrate of the lot. The entire lot goes from one process step to the next.

The following text describes the processes called out in the five figures.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

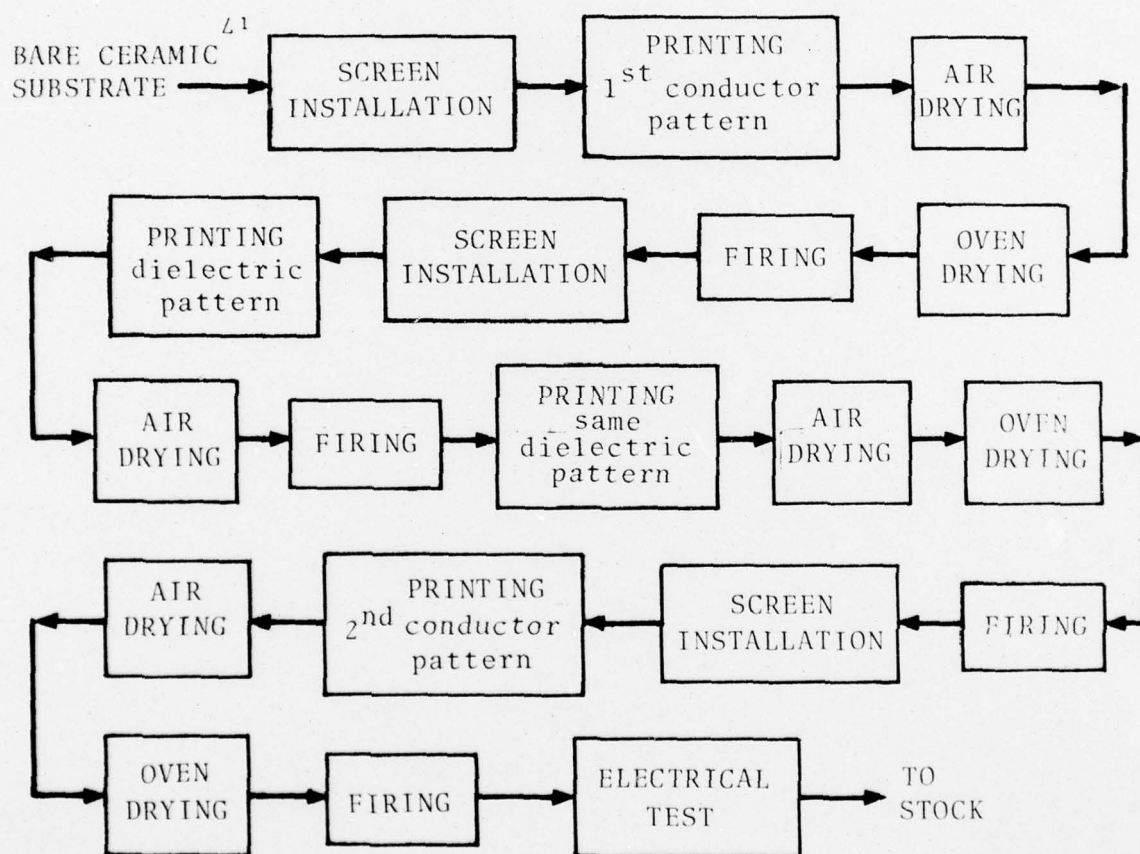


L1 When excessive amounts of foreign material are present on the substrate, a cleaning step is done first.

L2 The second resistor paste is printed before the first paste is fired. The two are fired simultaneously (called "co-firing"), because the first resistor values would be affected by a second firing.

Figure 6.2-3 SEQUENCE OF PROCESSES FOR SINGLE LAYER THICK FILM SUBSTRATE

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION



L1 When excessive amounts of foreign material are present on the substrate, a cleaning step is done first.

Figure 6.2-4 SEQUENCE OF PROCESSES FOR MULTILAYER THICK FILM SUBSTRATES USING DIELECTRIC CROSS-OVER BRIDGES

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

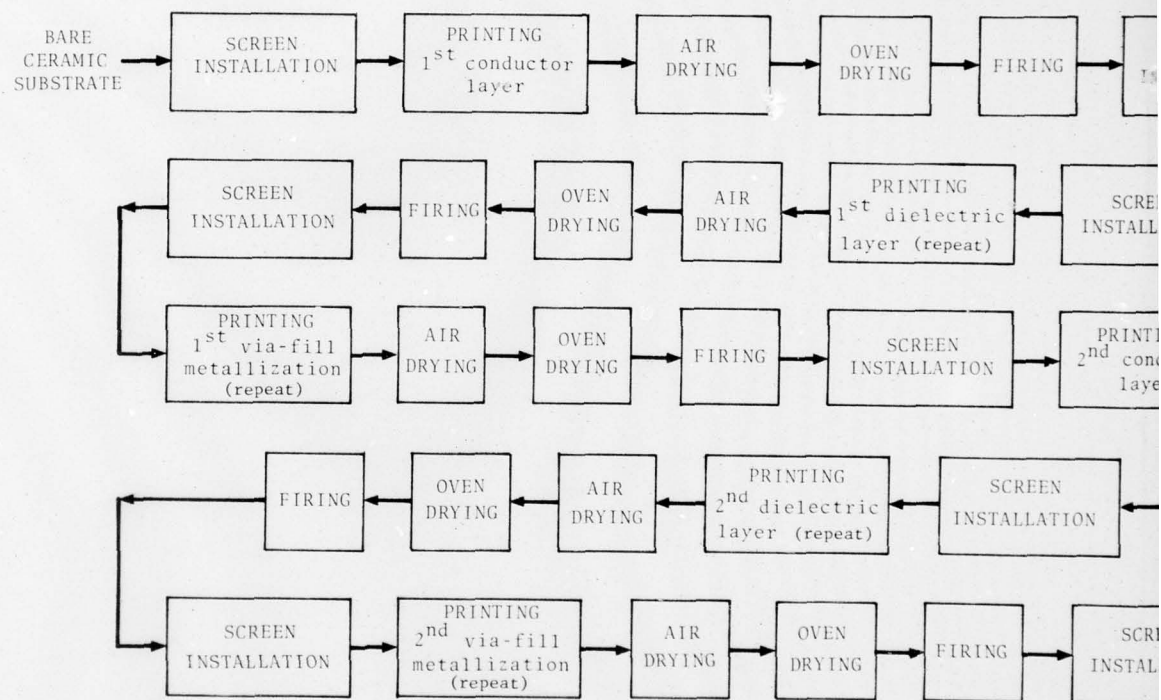


Figure 6.2-5 TYPICAL SEQUENCE OF THICK FILM FABRICATION

AD-A044 541

NORTHROP CORP HAWTHORNE CALIF ELECTRONICS DIV
DESIGN GUIDELINES FOR HYBRID MICROCIRCUITS. VOLUME II. ENGINEER--ETC(U)
MAY 77 T J AUBRY

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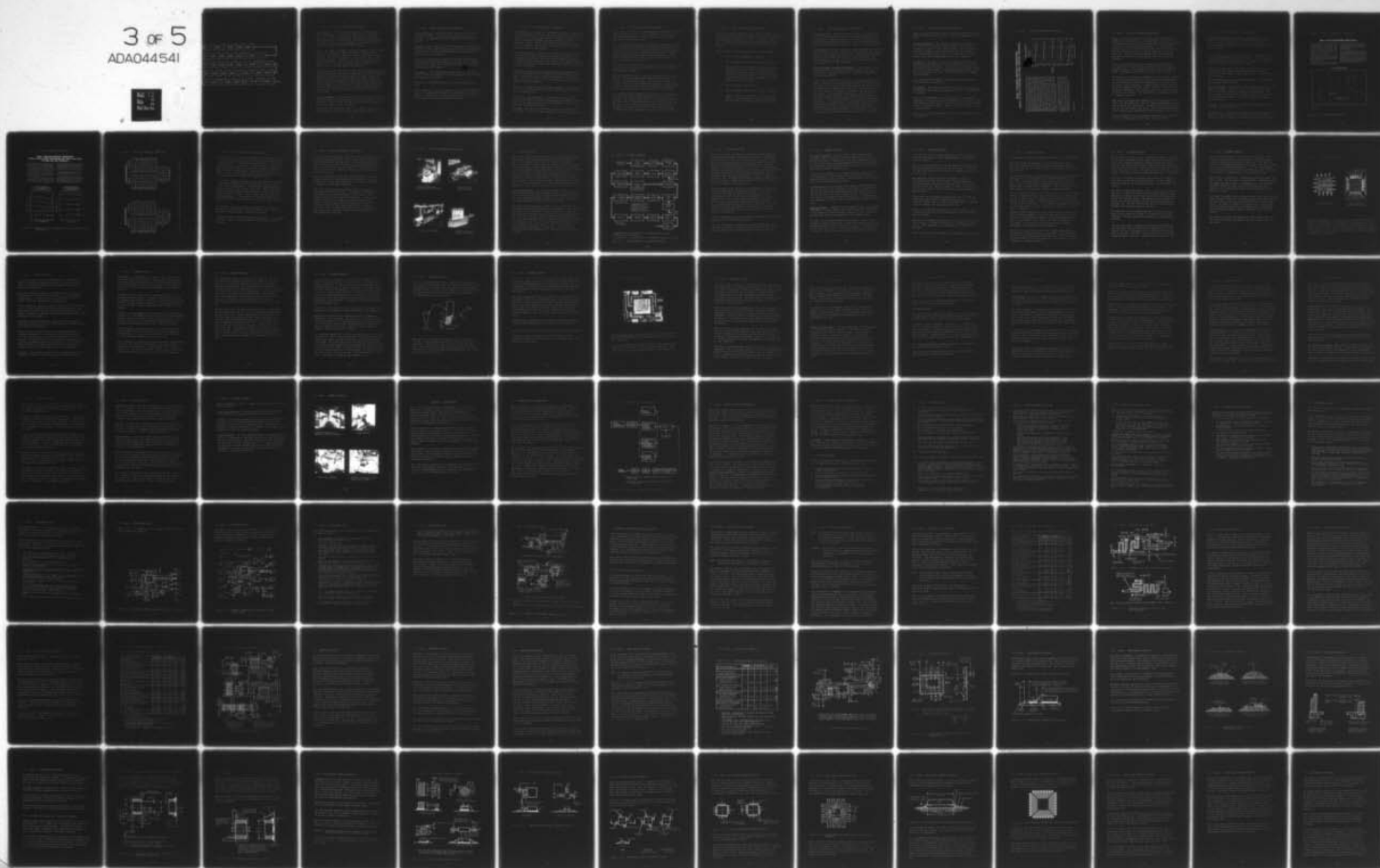
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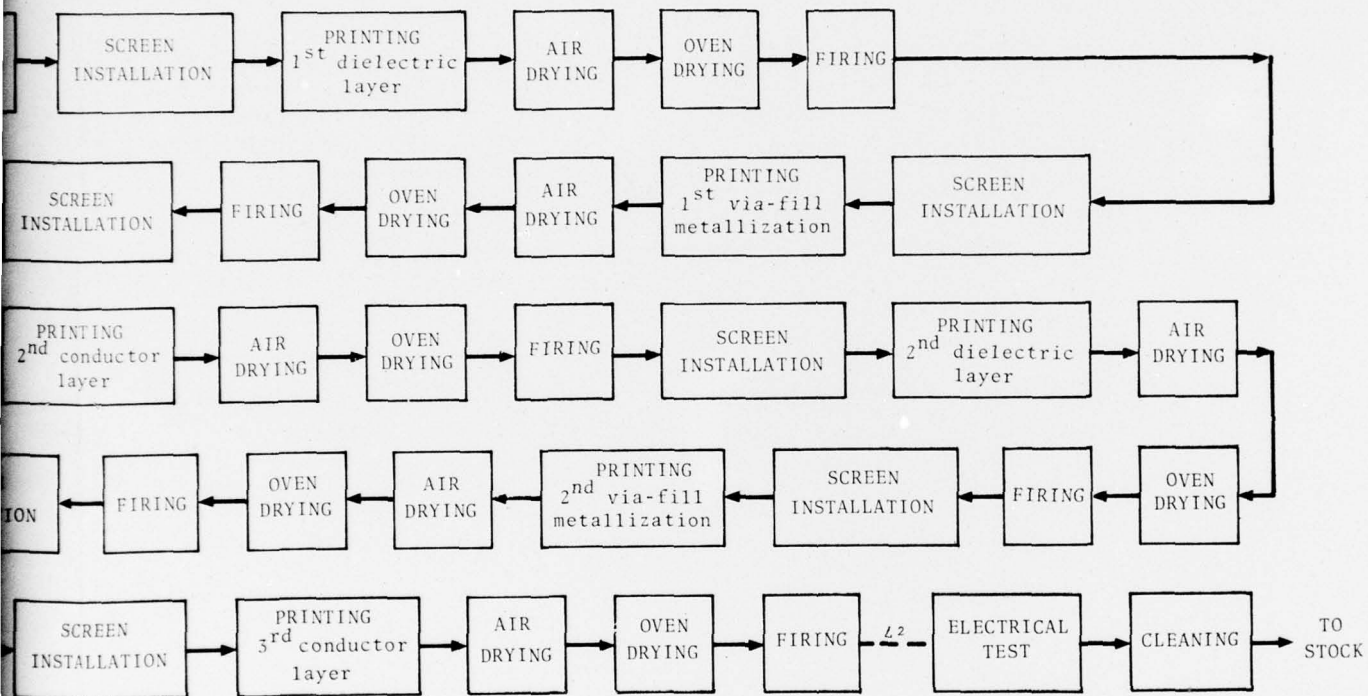
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6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Image Exposure. The screen used in thick film fabrication is steel or polyester mesh containing from 80 to 400 strands per inch. The screen is stretched on a metal frame that can be installed into the screen printer. The tension of the stretched screen must be above a certain minimum. The underside of the screen is coated with a photosensitive emulsion.

The 1x scale image is brought in contact with the screen emulsion; then using ultraviolet light, the image is exposed in the emulsion. The emulsion polymerizes wherever the light strikes. Since the emulsion is a negative type, the image film is light-field, right-reading emulsion. Close contact between film and emulsion as well as correct exposure time are important to create a sharply defined image in the emulsion.

Although the printer provides the capability of manually adjusting the screen location, each screen within one set (for one substrate) should have its image located to match the others in the set. Accurate placement of the image within the frame minimizes the need for manual adjustments later during the screen installation and set-up process. Criteria for the image exposure process are intimate contact between the film and screen emulsion, correct exposure time, and proper location of the image with respect to the frame.

Image Development. After exposure the screen emulsion is developed in warm running water which dissolves the non-polymerized emulsion. This removes emulsion only from the area defining the pattern of paste to be applied to the substrate.

Criteria for the development process are complete removal of the non-polymerized emulsion to achieve good image resolution.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Visual Inspection. Inspection at this point checks for image resolution, pinholes in the remaining emulsion, location of the image, and complete removal of emulsion within the image pattern.

Block-Out. When inspection of the developed screen reveals pin holes or any other undesirable open areas in the emulsion, these openings can be closed by hand-painting with blockout solution which dries in 3 to 5 minutes.

Criteria for the block-out process are careful application of the solution to avoid spreading into the image areas, complete closure of the undesirable openings, and control of the amount of solution to avoid lumps.

Oven Drying. After developing, the emulsion is oven dried at $\approx 35^{\circ}\text{C}$ in order to harden it to its full strength, and to ensure its adhesion to the screen.

Criteria for the baking process are correct temperature and time.

After baking, the screens are ready to be used in the printing process. The emulsion can later be removed and a new emulsion applied, permitting the screen preparation processes to be performed again to create a new image on a screen.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Screen Mounting. In many screen printers the screen is mounted to the printer using only screws. The clearance holes for the screws are not close fitting to the shaft of the screws and thus do not provide repeatable alignment for each subsequent screen. X, Y and rotary (called "Theta") adjustment screws provide the capability to manually adjust each screen position after the screen has been mounted on the machine.

Certain manufacturer's machines in addition to mounting screws, have guide pins that fit into holes in the screen frame. The close tolerance mating of the pins and holes provide repeatable alignment of each subsequent screen frame. Other methods (instead of guide pins) have also been used to provide repeatable location of each screen frame.

Repeatable-screen-location within the machine does not eliminate the need to adjust the first screen to the first substrate. It does eliminate the need to repeat the adjustment for each subsequent screen in the same set. (A set consists of all the screens required for one substrate.)

Figure 6.2-2 shows the screen alignment procedure. This procedure may be necessary only once per set of screens or once per each screen within the set.

Criteria for screen mounting are proper mating of the screen frame to the mounting surface in the machine, and complete tightening of the mounting screws to prevent movement of the screen after the printing cycle begins.

Printing. This process is sometimes called "Screen Printing" or "Screening." The bare ceramic substrate is placed in position and

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

held in place by vacuum. Rectangular shaped substrates are usually butted against stops on two sides, making it easy to slide the substrate into position. Curved substrates usually require some unique locating provisions.

It is important that the paste be completely homogeneous. Uneven distribution of particles within the paste will change the resistivity. Before each use, the paste should be stirred thoroughly. (Placing the paste jar on constantly moving rollers is unsatisfactory, because the net result is that the particles in the paste are being ball-milled down to smaller and smaller sizes. This also changes the resistivity.)

The paste to be printed on the substrate either flows automatically from a reservoir to the top side of the screen or is manually applied using a spatula.

When the actuating switch is pressed, the printing cycle begins with the substrate-holding-platform moving forward under the screen. The squeegee then moves across the top surface of the screen, forcing the paste through the open areas in the screen emulsion. The paste being squeezed through the openings adheres to the substrate forming the image pattern on the substrate.

The substrate-holding-platform then returns to its starting position where the newly printed substrate is accessible to the operator. The squeegee moves back to its starting position at one end of the screen, pushing the remaining paste also to that end of the screen. Now - platform, squeegee, and paste are all in position to begin the next cycle. The printed substrate is removed and a bare substrate is placed in position. Before

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

removal, the printed substrate can be inspected under a microscope. Some screen printing machines can be set to automatically eject the printed substrate. In such an automatic mode, it is very efficient to have the substrates ejected onto a conveyor belt. The wet paste can be air dried and oven dried on the conveyor.

Primary criteria for the printing process are as follows:

1. Correct image alignment to substrate.
2. Close parallelism of screen to substrate surface.
3. Proper pressure of squeegee on screen and resultant pressure of screen on substrate. Sometimes the screen does not make contact to the substrate; in which case, the space between is critical. Excess squeegee pressure can cause the pattern to spread excessively on the substrate.
4. Proper tension of the screen.
5. Proper squeegee speed, hardness, angle of squeegee.
6. Proper viscosity of the paste to suit the screen mesh size, the speed and pressure of the squeegee, and the width of the pattern lines being printed.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Visual Inspection. After the printing of the first substrate in the lot, visual inspection looks for improper alignment of image to substrate, incomplete coverage of the image area, and excess paste spreading beyond the image size. This inspection should be performed periodically as the lot of substrates is being printed.

Paste Removal. If visual inspection reveals that the newly printed wet paste is unacceptable, the paste can be wiped off the substrate using a solvent-soaked lint-free wiper. (These wipers containing gold paste can later be processed to reclaim the gold.) The solvent evaporates quickly in open air, and a new paste pattern can be applied to the same substrate.

Screen Alignment and Machine Adjustments. If the image is not properly aligned to the substrate, the location of the screen in the machine is modified using the X, Y, and Theta adjustment screws in the machine.

If the image is defective in other ways, various adjustments may be needed. The cause of the defect must be judged by the operator. Excessively low viscosity and/or high squeegee pressure may cause the image lines to spread on the substrate. Excessively high viscosity and/or low squeegee pressure may cause the image to be interrupted. Non uniform printing may be caused by lack of parallelism and/or too large a gap between the screen and the substrate. These are only examples of the causes of defective print images. The sequence of Paste Removal, Screen Alignment and Machine Adjustment, Printing, and Visual Inspection is repeated as many times as necessary to achieve good image definition along with proper alignment on the substrate. If the image on each screen has been previously located to match the

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

image in each of the other screens in the set, then this repeated sequence should only be necessary on the first substrate of the lot.

Screen Installation. This process, called out in Figures 6.2-3, 6.2-4, and 6.2-5, can be the entire sequence (and repeated sequences) of process steps shown in Figure 6.2-2; but usually the entire sequence is only required on the first screen of a set. When another screen of the set is installed, it usually requires only slight adjustment of the image alignment.

Air Drying. This process consists of simply allowing the wet paste on the substrate to dry at room temperature in open air for approximately 10 minutes. This process is needed to permit the drying to begin slowly. Accelerated drying of newly applied paste can create a dry film on the surface only while trapping solvents below.

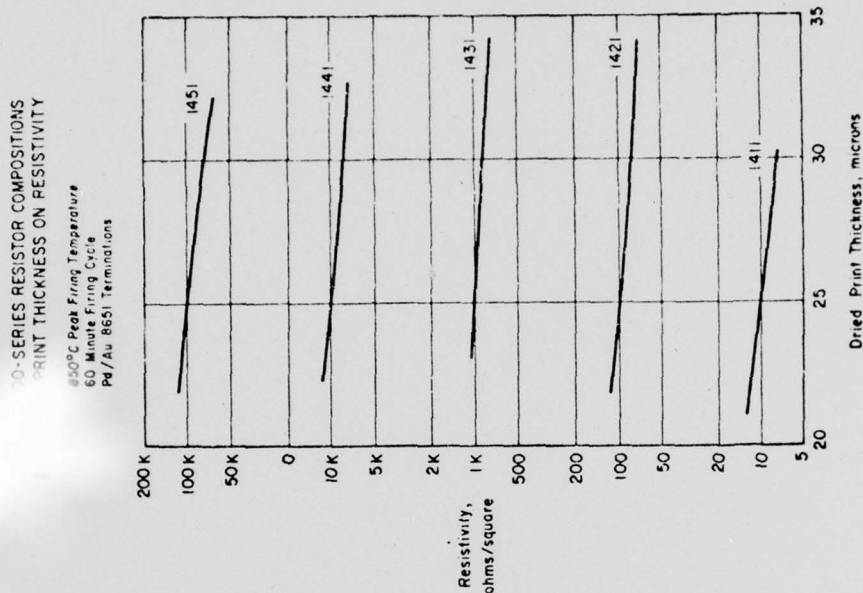
The criterion for air drying is that the paste surface has had sufficient time to level out.

Oven Drying. This process accelerates the drying. It consists of baking the substrates at approximately 125°C for approximately 10 minutes.

The dry film thickness of resistive pastes has an important influence on the resistivity of the material after firing. Paste manufacturers usually specify the effect of the dry film thickness on the as-fired-resistivity. Figure 6.2-6 is an example of such a specification.

The criteria for oven drying thick film paste is that the paste be thoroughly dry.

BIROX* 1400-SERIES RESISTOR COMPOSITIONS EFFECT OF PRINT THICKNESS ON FIRED RESISTOR PROPERTIES



Control and reproducibility of resistor print thickness is essential to obtaining predictable, reproducible fired resistor properties. The recommended dried print thickness for 1400-Series resistor compositions is 25 microns, and satisfactory results can generally be obtained with dried print thicknesses of 22-28 microns. Changes in average resistor print thickness or widely varying print thickness, however, cause corresponding variations in resistivity, TCR, and other fired resistor properties. The recommended print thickness can normally be obtained and consistently maintained when a quality automatic or semiautomatic screen printer and quality 200-mesh stainless steel screens (0.7-mil emulsion thickness) are used. Compromising the quality of either the printer or the screen generally compromises the performance and consistency of the fired resistors as well.

The information presented is based on evaluations of 1400-Series resistor compositions and is believed to be typical of these materials. This information can be useful both in predicting the effect of print thickness variations on resistivity and TCR and determining the probable cause of unexpected changes in fired resistor properties.

*Reg. U.S. Pat. Off.

Figure 6.2-6 EFFECT OF DRIED PRINT THICKNESS ON RESISTIVITY

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Firing. After the printed paste has been dried the substrate is ready for the firing process. The substrates are placed on the continuously moving belt of the furnace which carries them through the various heat zones inside the furnace. The furnace heat evaporates all the organic material in the paste and causes the metallic and glass particles to fuse to each other and to the substrate. When the substrates emerge, they can be manually unloaded from the belt or permitted to fall off the end into a container.

Thick film furnaces have three to twelve separate heat zones. The substrates carried through the temperature zones reach, in graduated steps, a peak temperature in the range from 500°C to 1000°C, depending on the particular paste on the substrate.

The usual way of checking the temperatures within the belt furnace is to place a thermocouple on the belt and as the thermocouple is carried through the furnace the temperature at any point within the furnace can be measured. A graph of temperatures within the furnace is commonly called the furnace "profile." The process of measuring temperatures and adjusting (where necessary) is called "profiling the furnace." One manufacturer's recommended profile is shown in Figure 6.2-7.

Many thick film pastes are intended to be fired in an air atmosphere, but when necessary, inert or reducing atmospheres can usually be piped into the furnace. Nitrogen, forming gas, and hydrogen are the most common gases used. (The use of hydrogen necessitates careful safety precautions because hydrogen is so volatile.)

Safety precautions are also important whenever berylia substrates are to be fired because berylia fumes are highly toxic.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

When the furnace profile is changed, several hours are usually required for the new profile to be reached and stabilized. For this reason paste manufacturers have produced conductive, resistive and dielectric materials that are all fired with the same furnace profile.

The as-fired resistivity of resistive paste is influenced by the peak firing temperature. Sheet resistivity is also affected by the length of time of the firing cycle. Figure 6.2-8 shows two graphs that depict one manufacturer's ratings.

The resistor temperature coefficient of resistance (TCR) is also influenced by both peak firing temperature and firing time. Figure 6.2-9 shows graphs of these two effects for five different paste materials.

The most important criteria for the firing process are the belt speed and the furnace profile.

Resistor Trimming. Laser trimming for thick film resistors is the same as described in Section 6.1. For resistors having widths >0.020 (0.508 mm), abrasive trimming can be performed. This process sprays a fine mesh grit through a small nozzle to "sand-blast" the resistor material. Abrasive trimming can produce accuracies of $\pm 5\%$.

Cleaning. The cleaning process for thick film substrates is the same as described in Section 6.1.

Electrical Test. The substrate electrical test called out in the multilayer flow diagrams is a continuity checkout, performed to detect any shorts or open circuits under the dielectric material.

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

BIROX[®] THICK FILM RESISTORS FIRING PROFILE

The standard BIROX[®] profile reproduced below is a 60 minute cycle with 9-10 minutes at a peak temperature of 850°C. There are three critical segments of the firing curve: 300°-450°C in the heating portion of the cycle where the organic binders are removed; the peak temperature range; and 600°-375°C in the cooling portion of the cycle, which is the annealing range.

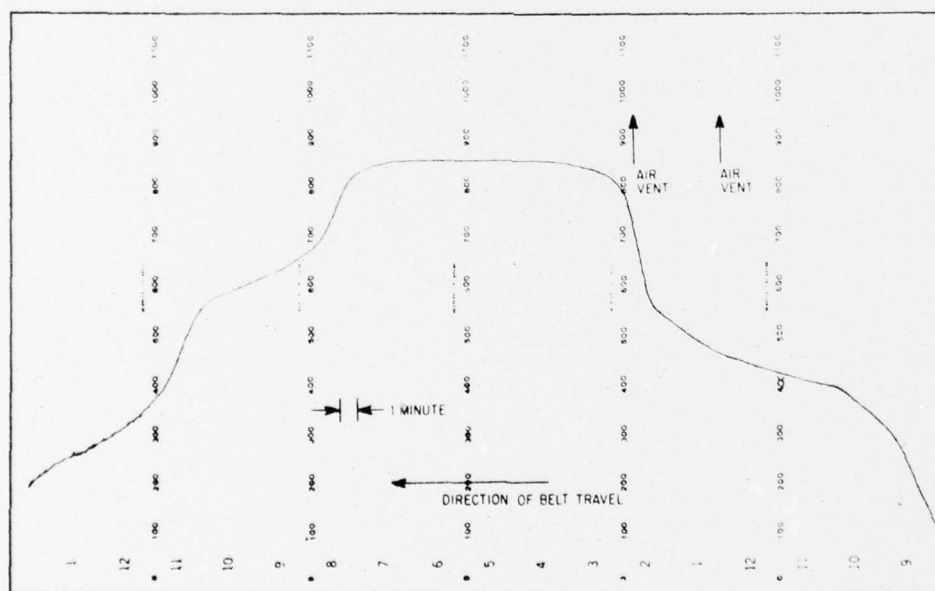
Heating rates in the 300°-450°C range should be slow enough to allow complete removal of organic materials before the glass in the composition softens. Heating rates should not exceed 60°C/minute in this range.

The peak firing temperature and time at temperature determine the resistivity and TCR of the fired

resistors. An increase in either temperature or time at peak causes a decrease in sheet resistivity. Increased temperature causes a positive change in TCR while increased time at peak shifts TCR in a negative direction.

It is important that the cooling rate in the temperature range between the softening point and annealing point of the glass (600°-375°C) be relatively slow (less than 60°C/minute). This allows residual stresses set up by the differences in expansion characteristics of the conducting and vitreous phases to be relieved while the glass is at relatively low viscosity. Very high cooling rates can lead to both erratic TCR's and stability problems.

TYPICAL FIRING PROFILE



Reg. U.S. Pat. Off.

Figure 6.2-7 TYPICAL FURNACE PROFILE

BIROX® 1400-SERIES RESISTOR COMPOSITIONS EFFECT OF PEAK FIRING TEMPERATURE AND FIRING CYCLE TIME ON FIRED RESISTOR PROPERTIES

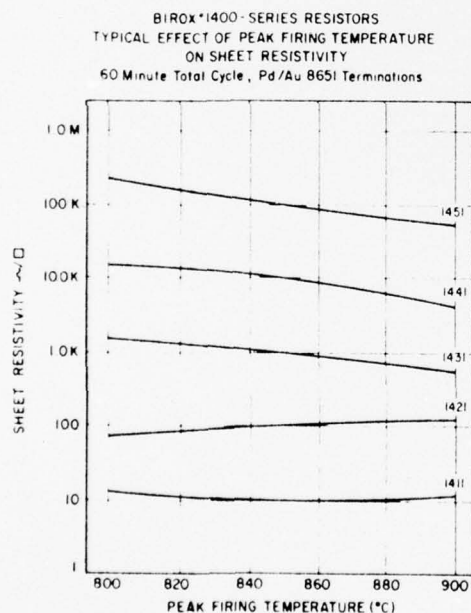
BIROX 1400 Series resistor compositions are formulated for firing in air through a belt furnace. A 60-minute cycle with a peak temperature of 850°C and a 9-10 minute soak is recommended. (See bulletin A 81927 for details.) Satisfactory results can be obtained when this firing schedule is modified, but the fired resistor properties — particularly resistivity and TCR — will vary from those obtained with the recommended peak firing temperature and firing cycle time.

The information presented shows the effects on resistivity and TCR of varying the peak temperature from 800° to 900°C and varying the belt speed to change the cycle time from 45 to 75

minutes. 1400 Series compositions are relatively insensitive to variation in the firing schedule, but this information confirms the necessity of control and reproducibility of firing conditions to obtain predictable, reproducible fired resistor properties.

The information presented is based on evaluations of BIROX 1400 Series resistor compositions and is believed to be typical of these materials.

The relationships depicted can be useful in predicting the results which will be obtained when the recommended firing schedule is not used, or alternatively, in determining the probable cause of unexpected changes in fired resistor properties.



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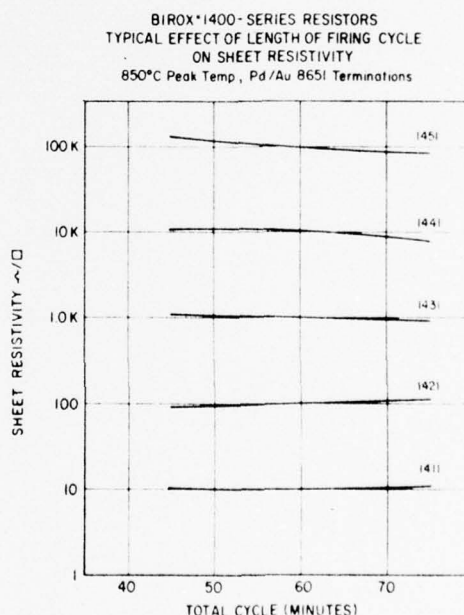


Figure 6.2-8 EFFECTS OF PEAK TEMPERATURE AND FIRING TIME ON SHEET RESISTIVITY

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

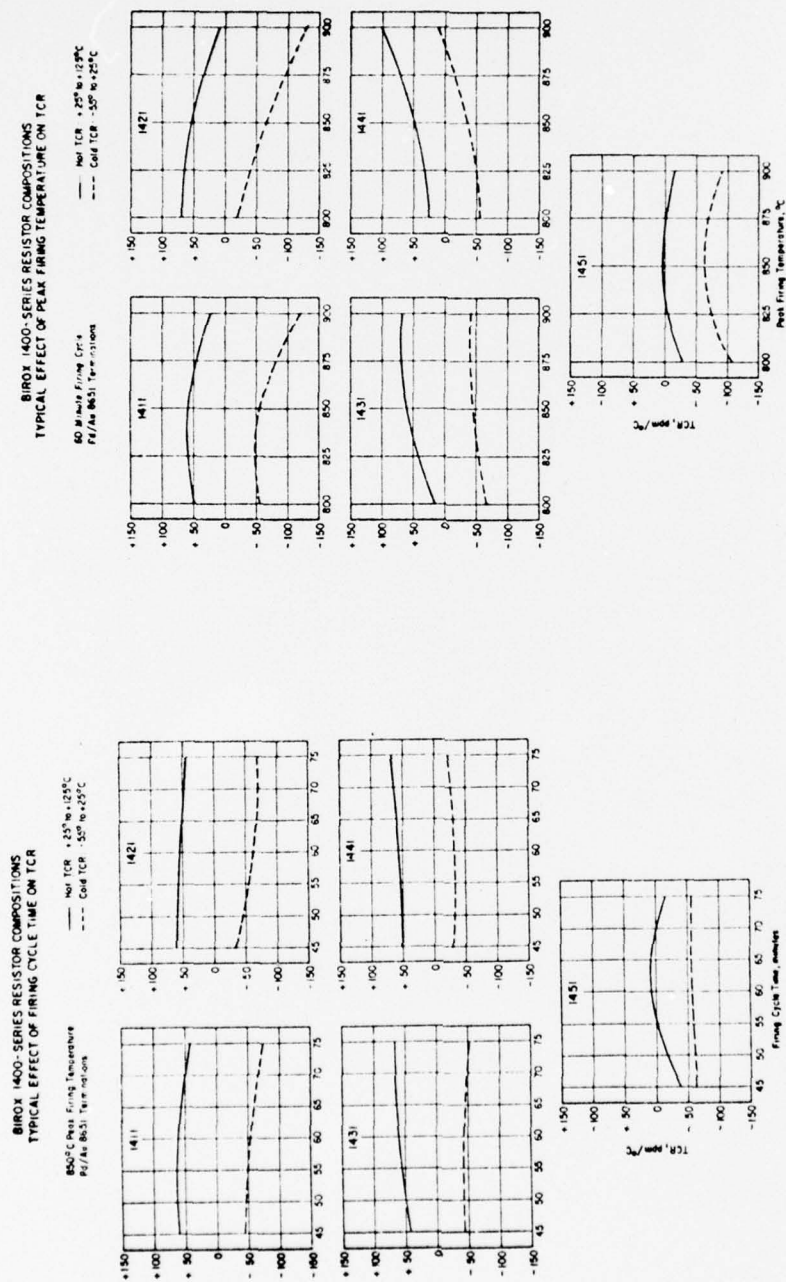


Figure 6.2-9 EFFECTS OF PEAK TEMPERATURE AND FIRING TIME ON RESISTOR TCR

6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

If the checkout is to be performed manually, two hand-held probes are placed at appropriate points on the conductor tracks and the connection or lack of connection between the two is indicated by a light or buzzer. Each probe is moved from place to place (as described on the probe list) and a reading taken at each place. Manual probing of approximately 1200 points can take up to 10 hours. A more complete description of manual continuity checkout is given in Section 4.3, Multilayer Substrate Tests.

If automatic checkout equipment is used, the substrate is placed in the fixture and multiple probes make contact to all the substrate points simultaneously. The automatic equipment compares each probe point to every other probe point. Older, continuity checkout equipment using stepping switches can check 1200 points in approximately 5 minutes. Newer, solid state equipment can perform much faster. A description of the relationship between the multiple probes and the substrate pattern is given in Section 4.3.

An important criterion for electrical testing is good contact between the probes and the substrate conductor tracks. This is important for both automatic and manual procedures.

In manual checkout, correct placement of the probes is an important criterion. (Errors typically increase as the operator becomes fatigued.)

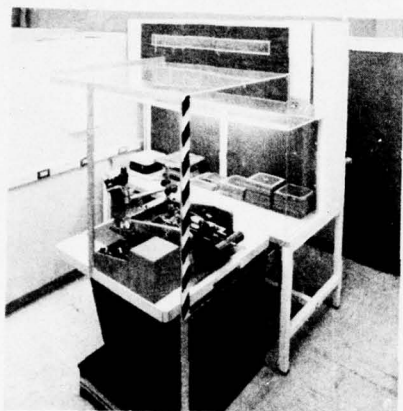
6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION

Resistors can be integral to a multilayer substrate, and when used are typically placed directly on the ceramic surface with their ends overlapping the conductor pads. It is preferred that the resistors be printed and fired last, because subsequent firing cycles would effect the resistor values. If they cannot be fired last, then that effect should have already been compensated in the resistor design.

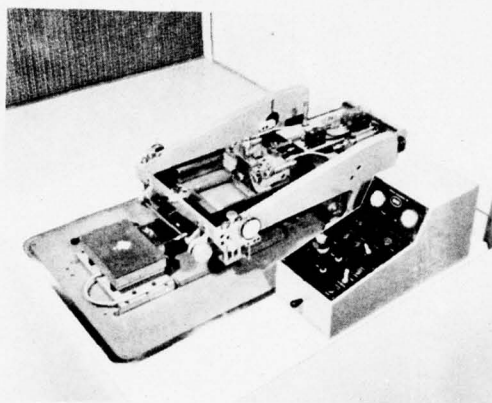
Thick film substrates can be fabricated as multiple, step-and-repeated images on a large ceramic as described for thin film. In that case a scribe and break process step would be performed to separate the individual substrates.

Many thick film pastes are described by their manufacturer as being capable of being co-fired. This means, for example, that the double screen for the dielectric layers could be fired together instead of two separate firing steps. In high volume production any such co-firing can be significant, but for smaller quantities many substrate manufacturing groups prefer to "play it safe" and fire each screened paste separately. Since the furnace is never turned off, and the furnace belt is constantly moving, the time required to load and unload is the only operator time involved.

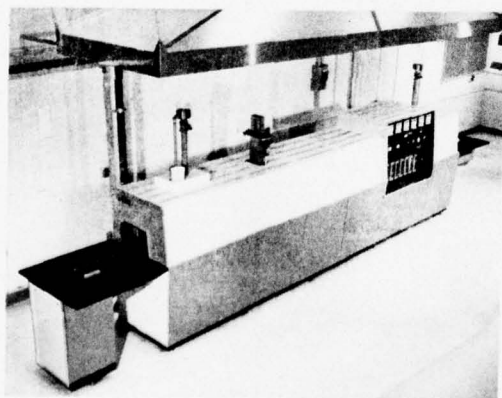
6.2 (Cont.) THICK FILM SUBSTRATE FABRICATION



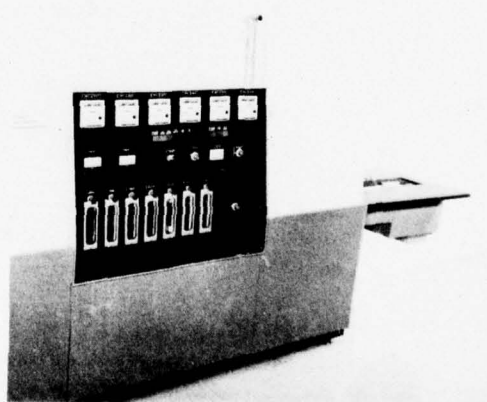
SCREEN PRINTER WITH
LAMINAR-FLOW CLEAN BENCH



CLOSE VIEW OF
SCREEN PRINTER



6-ZONE BELT FURNACE



CONTROL PANEL FOR
6-ZONE BELT FURNACE

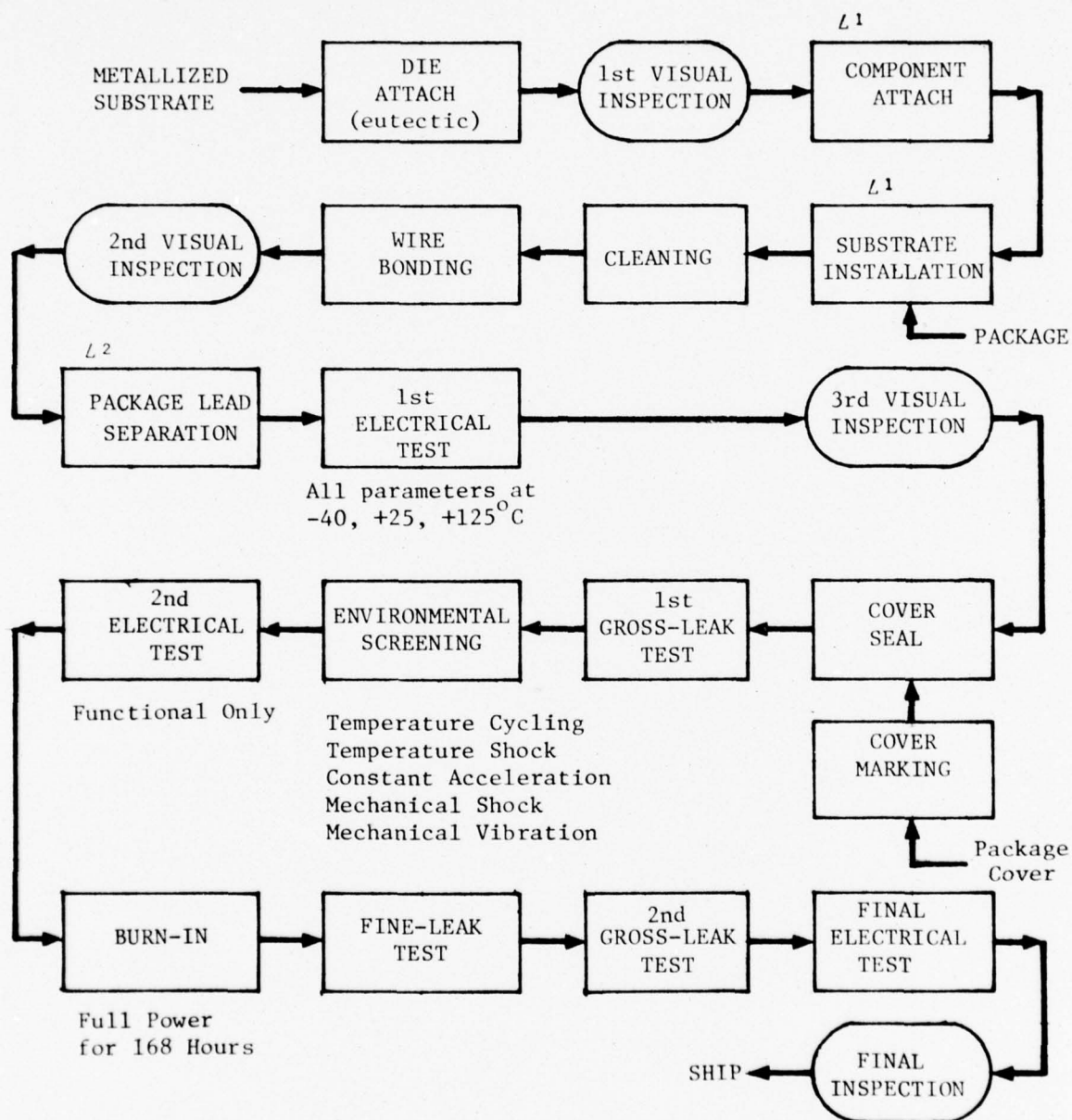
6.3 ASSEMBLY PROCESSES

This section describes assembly processes performed after substrate fabrication. Where differences exist due to thick or thin film they will be pointed out in the text. Figure 6.3-1 shows a typical sequence of assembly steps for a high reliability hybrid. The sequence shown for attachment and installation processes may be reversed depending on the temperatures involved. Each subsequent process should be at a temperature lower than previous ones in order not to adversely affect prior attachment materials. This consecutive lowering of temperatures is referred to as "temperature stepping." To avoid dust and other contaminants, all assembly processes should be performed in a clean-room environment, and laminar flow clean benches are often used inside the clean room.

Die Attach (eutectic). The eutectic attachment process is performed primarily on silicon semiconductor and resistor chips (or dice) to attach them directly to the substrate mounting pads without using additional bonding material, and to obtain good contact for thermal transfer from the die to the substrate.

The eutectic-attach equipment provides a tray on which the dice are placed and a holding platform for the substrate. The tray and platform are on a frame that can rotate similar to a carousel. This frame can be rotated back and forth by the operator to bring first the tray, then the platform, under the installation tool. The tip of the installation tool is commonly called either a "quill" or "capillary." The size of the capillary must be only slightly larger than the die it will pick up. Various size capillaries can be mounted simultaneously to the tool. The tool can be rotated to bring the appropriate size capillary into the working position.

6.3 (Cont.) ASSEMBLY PROCESSES



^{L1} Component Attach and Substrate Installation are often done in reverse sequence.

^{L2} This process is required only for packages having lead frames.

Figure 6.3-1 TYPICAL SEQUENCE OF ASSEMBLY PROCESSES

6.3 (Cont.) ASSEMBLY PROCESSES

With the tray under the capillary, and with the appropriate die in the proper orientation, the operator actuates a switch which causes the tool to lower and pick up the die by suction. When the die has been raised from the tray, the operator rotates the frame and the platform holding the substrate comes under the capillary. Then when the substrate is in proper orientation and position, the operator actuates a switch which causes the capillary to lower the die down to the substrate mounting pad. The tool then moves back and forth approximately 5 mils (0.127 mm) for several cycles; "scrubbing" the bottom of the die on the mounting pad. The suction is then released and the tool lifts, leaving the die attached to the mounting pad.

The temperature of the capillary is approximately 430°C and the substrate temperature is approximately 330°C . These temperatures along with the friction caused by the scrubbing create a temperature of 370°C at the interface between the die and mounting pad. This is the eutectic temperature of gold/silicon and an alloying takes place between the silicon and gold. The die is usually purchased with gold on its back side. This gold backing facilitates the eutectic attach process because some of the gold is diffused into the silicon, thereby giving the process a "head start."

Eutectic attachment is easier on thin film gold than on the mixed gold and glass of thick film materials.

Criteria for eutectic attachment are control of the tool and substrate temperatures, correct location and orientation of each die, and proper size relationship between capillary and die.

6.3 (Cont.) ASSEMBLY PROCESSES

1st Visual Inspection. An inspection is needed after eutectic attachment because if rework is required the rework will be performed at the eutectic temperature. This high temperature cannot be applied after other lower temperature processes have been done. This inspection looks for proper eutectic melting of the materials; indicated by "wetting" around the die.

A eutectically attached die is usually removed by twisting it off its mounting pad. When twisted, the die often breaks leaving portions attached to the substrate. These portions can be chipped away to make the mounting pad reusable.

If the mounting pad is unusable after removing the original die, then the new die can be eutectically attached to a moly-tab and the moly-tab epoxied to the mounting pad. The epoxy, of course, can only be used if the specifications permit. The moly-tab is used because it spreads the heat from the die. This heat spreading compensates for some of the low heat transfer property of the epoxy.

Component Attach. Conductive or nonconductive epoxy for component attachment is usually applied only to the substrate. However when a large amount is needed for heavy components (such as toroids) an additional amount can be applied to the component also.

The epoxy can be manually applied to the mounting pads or epoxy dispensing machines can be used. Dispensing machines typically use pneumatic pressure to bring epoxy from a reservoir through a needle to the substrate surface. The amount dispensed in one cycle can be adjusted. Epoxy can also be screen printed on the substrate

6.3 (Cont.) ASSEMBLY PROCESSES

using the same type of screens and printers used for thick film substrate fabrication. This technique applies a thin uniform pattern of epoxy.

Epoxy is typically applied to all the appropriate mounting pads, then the components are placed on top of the epoxy. The epoxy is then either oven cured or cured in air depending on the type of epoxy used.

The important criteria for epoxy attachment is control of the amount of epoxy and the proper time and temperature for oven curing. Since during the oven curing the viscosity usually becomes low, excessive amounts of epoxy or an excess of time at low viscosity can cause the epoxy to spread beyond the mounting pads.

Solder makes an intermetallic bond with the metal of both the component terminals and the substrate mounting pads. For this reason the solder tends to remain on the mounting pad. However, excessive amounts will spread beyond the pads.

Solder can be obtained in shapes cut from thin sheets. These "preforms" can be laid on the substrate pads and the components placed over them.

Another way of applying the solder is to "pre-tin" the metal parts. This consists of dipping the substrate or component into molten solder. Many components can be purchased with solder-coated terminals.

Solder paste can also be applied to the mounting pads. The paste

6.3 (Cont.) ASSEMBLY PROCESSES

can be manually applied, dispensed by a machine, or screen printed.

After the solder and components are in position, the entire substrate is then raised to the solder melting temperature and when the solder melts it bonds to both the component and the substrate metal.

One potential problem is that when the solder melts, the components sometimes float on the molten solder and thereby change their positions. A holding fixture can be used to prevent this movement. Such a fixture can be any nonsolderable sheet material having holes the shape of the components. Such a stencil fixture, when clamped to the substrate, prevents component movement.

Oxides on the metal surfaces or on the surface of the solder inhibit the solder from "wetting." Fluxes can be used, but attention must be paid to using fluxes with minimal corrosivity and to complete removal of any residuals. Another method used is to raise the temperature while the substrate is in a reducing atmosphere which chemically breaks down the oxide. Forming gas or hydrogen can provide such an atmosphere.

Hydrogen flame equipment can be used in the solder-attach process. Belt soldering equipment is also available which carries the substrates on a belt through a chamber of reducing atmosphere and while in the chamber, raises them to the melting temperature of the solder. The thick film firing furnace using a reducing atmosphere can also be used for this purpose.

Criteria for solder-attach are correct component placement and orientation, and proper wetting of the solder. High reliability specifications usually dictate that there be a fillet of solder or epoxy around at least three-quarters of the periphery of each component or component terminal.

6.3 (Cont.) ASSEMBLY PROCESSES

Beam-leaded chips require unique attachment techniques. The chip is the usual semiconductor chip except that the metal pattern on top is gold, and the terminals, instead of being flat on the surface, have integral gold ribbon leads that extend, like beams, over the edge of the chip. These beam-leads are usually 0.5 mils (0.0127 mm) thick, 3 mils (0.075 mm) to 5 mils (0.127 mm) wide and extend 5 to 8 mils (0.13 to 0.2 mm) beyond the edges of the chip.

The chip is intended to be mounted face down by TC bonding its beam leads on the substrate mounting pads. A wobble bonder is typically used for the attachment process. The procedure is as follows:

The chip is placed face down on a tray. In the tip of the bonding tool is a cavity the shape of the chip but slightly larger. The tool is lowered over the chip so that the body of the chip is nested into the tool cavity. The beams do not go inside the cavity, but extend beyond the cavity across the bottom face of the tool tip. The tool picks up the chip by exerting suction through a hole down the center of the tool.

The substrate is then brought under the tool and positioned so that the chip beams are aligned to the mounting pads on the substrate. The tool lowers until the beams are contacting the substrate.

The tool then exerts a downward force, pressing the beams on the substrate. The tool then tilts to approximately 1° from vertical so that the downward force is applied by only one side of the tool. The force is now exerted only on the beams along one edge of the chip. The tilt is then rotated to the

6.3 (Cont.) ASSEMBLY PROCESSES

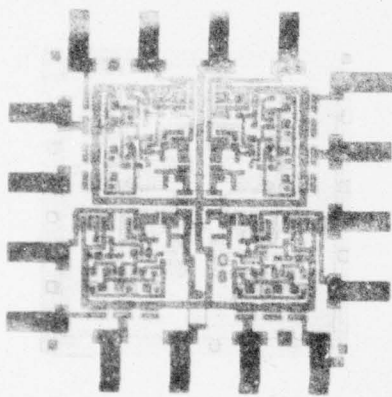
next set of beams along the adjacent edge of the chip. This rotating tilt proceeds to all four edges of the chip exerting a force on only one set of beams at one time. Since the tilt rotates in a continuous motion the outer edge of the tool actually rolls across each beam individually. It is this wobble motion of the rotating tilt which gives the bonder its name. The wobble cycle usually is repeated several times around the chip.

The tool tip is typically at a temperature within the range from 320 to 450°C. The substrate is maintained at a temperature within the range from 280 to 350°C. The downward force of the bonder should be within the range from 20 to 100 grams per beam. Excessive force can break the beams or the connections of the beams to the chip.

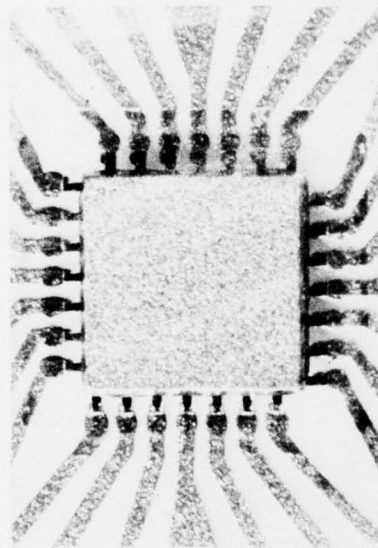
Beam lead TC bonding is more effective on thin film than on thick film substrates because of the higher purity of the thin film gold. Multilayer thick films give less reliable bonds than do single layers. But there is evidence that by abrasively cleaning the thick film mounting pads prior to bonding, much stronger bonds can be produced on either single or multilayer thick film substrates.

The criteria for beam lead bonding are proper temperatures for the tool and substrate and adequate but not excessive force on the beams.

6.3 (Cont.) ASSEMBLY PROCESSES



BEAM LEADED CHIP



BEAM LEADED CHIP
BONDED ON SUBSTRATE

Substrate Installation. Excluding eutectic attachment, the installation of the substrate in the package can be done before or after components are attached. The sequence is usually dependent on the temperatures involved. However, the sequence is sometimes influenced by a decision to perform certain electrical tests before committing the substrate to the package.

6.5 (Cont.) ASSEMBLY PROCESSES

If electrical tests are to be performed prior to installation, then wire bonding of components only must also precede installation. Wire bonding from substrate to package leads would be done after installation.

Epoxy can be manually applied or dispensed onto the surface of the package base. Solder can be applied as a paste or in pre-formed shapes. In order to solder the substrate in place the bottom side of the substrate must be metallized.

If the package has side walls, there is little or no concern about epoxy or solder spreading, but when platform packages are used (which have no walls) care must be exercised to prevent the solder or epoxy from spreading into the cover mounting areas around the edges of the package.

Avoiding air pockets between the substrate and the package is important; particularly when good heat transfer is necessary from the substrate to the package.

Another method(not widely used) for substrate installation and component attachment is to attach using thin teflon preforms. By a specialized process, the teflon is caused to act as an adhesive. Although teflon is not an electrical conductor and does not have good thermal conductivity properties, it does permit an indefinite number of reworks and does not have the long-term harmful effects that other organics have on semiconductors.

Cleaning. The important criteria for any cleaning process after soldering is that the solder flux must be thoroughly removed.

6.3 (Cont.) ASSEMBLY PROCESSES

Wire Bonding. Three methods are commonly used to install interconnecting wires within a hybrid. The two most common methods are thermo-compression bonding (called "TC" bonding) and ultrasonic bonding (often called "stitch bonding"). The third is to solder wires by the usual assembly techniques of applying heat and flux.

TC bonding installs each end of an uninsulated gold wire by applying heat and pressure. Ultrasonic bonding installs either an aluminum (most common) or gold wire by scrubbing the wire ends into place at an ultrasonic frequency. For ultrasonic bonding of gold some heat is usually applied but not as much as for TC bonding.

Either TC or stitch-bonding can be performed on both the aluminum terminals of a semiconductor chip and the gold of the substrate and package. However, TC bonds on thick film gold are not as effective because of the glass mixed in the thick film material. Ultrasonic gold bonding on thick film is quite satisfactory.

The most commonly used wire diameter is 1 mil (0.025 mm), but larger diameters up to 10 mils (0.254 mm) can be accommodated with the proper size tool. Smaller wire (0.7 mil, 0.0178 mm) is being used more frequently for very small dice.

The TC bonder has a pedestal to hold the substrate and the bonding tool has a cone shaped tip that points toward this pedestal. The flat bottom of the cone tip is approximately 7 mils (0.178 mm) diameter for 1 mil (0.0127 mm) wire. The gold wire is fed, from a spool, down through a hole in the center of the bonding tip.

6.3 (Cont.) ASSEMBLY PROCESSES

Using a hydrogen flame, or electronic arc flame-off, the end of the gold wire protruding from the tool is melted to form a ball that is 2 to 5 times the diameter of the wire. The operator manipulates the pedestal location through the motion-reduction linkage (reduction ratio approximately 6 to 1). When the substrate is in the correct position, the bonding tip is lowered until the gold ball is contacting the appropriate pad. The tool then exerts a predetermined force on the gold ball (60 grams for 1 mil wire). This force, along with the heat from the tip (approximately 450°C) bonds the ball to the surface it is touching.

The tool then lifts; but since the end of the wire is now bonded to the surface below, the wire is, in effect, drawn down through the tip of the tool. Further manipulation of the pedestal relocates the substrate to place the next bond pad under the tool. The tool lowers and repeats the bond cycle. Again the wire is drawn through the tool as the tool lifts. At this point in the process the flame is brought to the wire, slightly below the tip of the tool. The flame cuts the wire, and creates another ball on the end. The tool is now ready to begin another bonding cycle. Using a pair of tweezers, the operator pulls off the excess wire that remains attached to the bond pad after the flame cut.

6.3 (Cont.) ASSEMBLY PROCESSES

Also available is an automatic "tail puller." Operating in this mode, a clamping mechanism closes on the wire after the second bond has been made. As the tool rises the fact that the wire is clamped causes the wire to break at the edge of the bond; leaving no excess "tail" on the substrate. As the tool rises the flame (or arc) is actuated and a new ball is formed on the end of the wire. The clamp then releases the wire allowing it to be drawn into the capillary until the newly formed ball stops against the bottom side of the capillary. The bonder is then ready to begin the next bonding cycle.

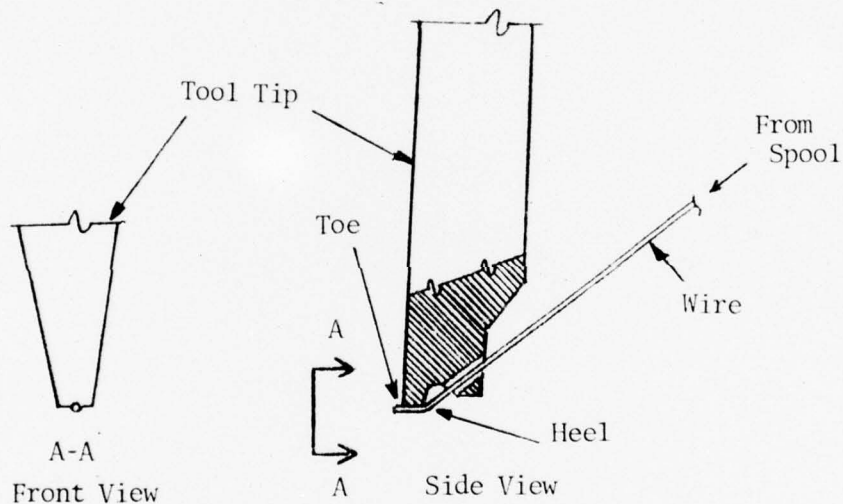
Criteria for TC bonding are correct location of each bond, clean bonding pads, and proper force and temperature of the bonding tool.

Equipment for ultrasonically bonding gold wire is similar in appearance to the TC border. The gold wire is fed through a hole in the cone-shaped tip. A hydrogen flame or electronic flame-off creates a ball on the wire end, and manipulation of either the substrate pedestal or the tool is through a motion reduction linkage. The differences are as follows:

The substrate temperature is within the range from 25 to 200°C, the tool from 25 - 250°C. When the gold ball is pressed on the first bonding pad, ultrasonic vibration of the tool tip scrubs the ball on the pad. The second bond is made the same way, but when the second bond has been completed the tool breaks the wire at the edge of the bond so that there is a small protrusion of wire out of the tool tip, and no excess wire on the bond pad. The tool raises and the flame creates a ball on the end of the protruding wire. The tool is then ready to begin the next bonding cycle.

6.3 (Cont.) ASSEMBLY PROCESSES

Ultrasonic aluminum bonders have a substrate holding pedestal, but no heat is applied to either the substrate or the tool. The aluminum wire has no ball on the end; and is fed from a spool to the bottom face of the tool tip as shown in the following sketch. Between the spool and tip are wire clamps that control the wire movement after the second bond.



When the tool is lowered to the bonding pad a downward force of 25 grams is exerted which triggers the ultrasonic generator. The vibration is transmitted to the tool tip through a transducer arm. This ultrasonic vibration scrubs the aluminum wire on the mounting pad. The bond is made by the downward pressure and the heat generated by friction.

6.3 (Cont.) ASSEMBLY PROCESSES

Because the bonding face of the tool has only a half-round groove to partially guide the wire, the movement of the tool between the first and second bonds must be in a relatively straight line in a direction to cause the wire to slide straight through the groove. (Side movement of the tool would cause the wire to slip out of the groove.)

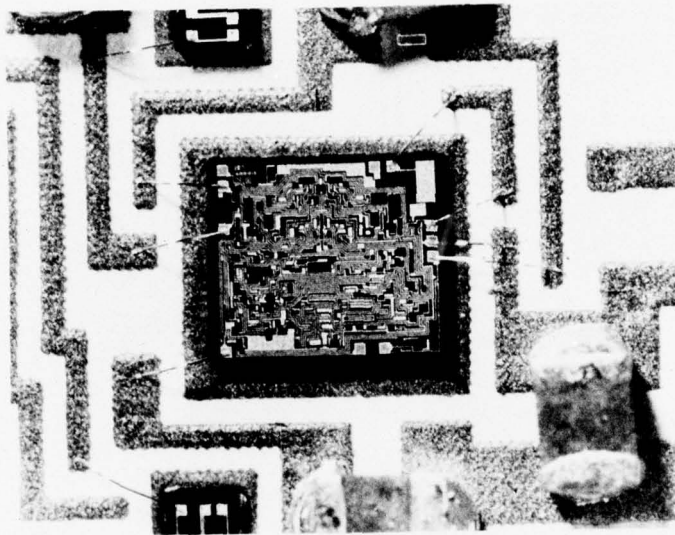
After the second bond is made, the heel of the tip knicks the wire in order to weaken it just behind the bond. With the clamps holding the wire, the tool moves up; thereby breaking the wire at the knick. The clamps then open, move back a predetermined distance, close on the wire, then move forward pushing the wire forward to protrude past the toe of the tip a distance of 1 to 3 times the wire diameter. The tool is then ready to begin the next bond cycle.

Because of the scrubbing action, ultrasonic bonding can usually break through contamination on the surface of the bond pad.

Glass on the surface of thick film pads can also be broken through.

Criteria for ultrasonic bonding are proper setting of the pressure and power controls for each of the two bonds, and correct location of each bond.

6.3 (Cont.) ASSEMBLY PROCESSES



2nd Visual Inspection. Inspection after wire bonding looks for correct component placement and orientation as well as correct wire connections.

If a wire is bonded incorrectly, the bonds usually cannot (and should not) be released. The wire must be pulled off. This typically leaves the bonded ends attached to the bonding pads.

6.3 (Cont.) ASSEMBLY PROCESSES

In spite of the fact that the bonding pads on many semiconductor chips are small a second bond can sometimes be made next to the first bond. Although it is physically possible to bond a second wire directly on top of the first bond, a second bond flat on the terminal pad is the only rebonding acceptable to high reliability specifications. Therefore when the acceptable second bond method cannot be used to rework an incorrect wire, the entire chip must be removed.

Replacing a eutectically attached chip after other components have been installed is a particular problem. Because the eutectic temperature is too high for the solder or epoxies used for other components, a new die cannot be eutectically attached to replace the old one. The new die can be "moly-tabbed" and replaced with solder or epoxy as previously described for reworking eutectic attachments.

Epoxy or solder-attached components can be removed by applying heat to the area of that component only, thus softening the bond of that component while avoiding heating the bonds of other components. Replacement with another component is accomplished by localized heating or by epoxy-attachment with air curing epoxy at room temperature.

One problem encountered when replacing a previously solder-attached component is that a large percentage of the gold in the mounting pad has been absorbed (called "leached") into the removed solder. There is sometimes insufficient gold remaining to perform a second solder-attach. In such a case epoxy must be substituted.

6.3 (Cont.) ASSEMBLY PROCESSES

High reliability specifications often dictate the maximum percentage of wires allowed to be reworked (10% is the usual maximum). Only 15 percent of the components may be replaced. (Rewiring due to component replacement does not count toward wire bond rework.) All rework (for whatever reason) must be accomplished by a maximum of two rework cycles.

If the density of the components and wiring is such that one component and its wires cannot be removed without the risk of damage to other wiring, then a visual inspection should be performed before wire bonding, and any necessary rework of dice performed at that time.

Package Lead Separation. The most common type of hybrid package is a flat package having side walls. Flat ribbon leads pass through the walls and are sealed to them. (This package is sometimes called a "butterfly package.") The leads are fabricated from one piece of thin metal (typically kovar) and the ends of the leads, outside the package, are left joined together by a bar of the original metal. (The leads plus the connecting bar are called the "lead frame.") When the package was being fabricated, the connecting bar made it possible to electroplate the lead frame as well to handle all the leads as a single unit, and later the bar helps prevent bending of the leads.

6.3 (Cont.) ASSEMBLY PROCESSES

This process step cuts off the connecting bar in order that electrical tests can be performed. Since the final length of the leads is typically required to be shorter than the as-purchased length, part of the leads are cut off with the bar. This process step usually includes substituting tape for the metal bar in order to continue to support the individual leads.

The criterion for the lead separation process is that the final length of the leads be per specification.

1st Electrical Test

For highly reliable hybrids it is common to test for all parameters at room temperature and at the high and low temperatures of the specifications. (-40 to +100°C are common requirements.)

If dynamic resistor trimming is necessary it is at this time that it is usually performed. Care must be exercised in placing the trimming probes inside the hybrid, because the small uninsulated wires and the unprotected components can be easily damaged. After trimming, a cleaning process is usually performed to remove any residue that might be present due to the trimming operation.

It is important that the electrical integrity of the hybrid be ascertained before sealing the cover.

Parts that fail the first electrical test can be reworked to remove and replace defective components.

6.3 (Cont.) ASSEMBLY PROCESSES

3rd Visual Inspection. This inspection checks for cleanliness and measures the package lead lengths. It also looks for any damage that might have been done during the electrical tests.

Cover Marking. The cover is usually marked prior to being sealed on the package because less care is needed in handling the cover individually compared to handling the package with its protruding leads.

The marking material is commonly epoxy ink capable of withstanding temperature extremes, solvents, human handling, and salt spray. The number of characters is sometimes limited by the size of the cover, but the desirable markings are part number, serial number, lot code, and some kind of package orientation mark (most commonly this is a dot located to identify pin number 1).

The process can be performed by any method or with any equipment that provides clearly legible characters and applies a sufficient amount of ink. Screen printing is often used for the characters being repeated on each cover, and a sequential rubber stamp for the serial numbers.

Cover Seal. Unless the subsequent temperature stresses can be imposed within an inert atmosphere, then the cover should be sealed before Environmental Screening and Burn-In. Those tests are harmful to many unprotected components if performed in air.

6.3 (Cont.) ASSEMBLY PROCESSES

The three common methods of attaching the cover to the package are epoxy bonding, soldering, or welding.

Epoxy can be applied in liquid form or as a picture frame shaped preform. The preform can be placed between the two surfaces to be joined then cured at the appropriate temperature. Liquid epoxy can be applied to the border of a flat cover by screen printing.

When the cover is soldered to the package no flux can be tolerated because flux, trapped inside the hybrid is very harmful to the components. Therefore, since flux cannot be used, the process must be performed in an inert or reducing atmosphere.

Package sealing equipment is available to perform either solder or weld-sealing within a controlled atmosphere. The seam-welding mechanisms are housed inside a sealed chamber into which the appropriate atmosphere is piped. A viewing window is provided, and sealed into the wall are rubber gloves that can be used to reach inside without disturbing the seal. The chamber also has a double-door air lock compartment through which all parts must pass in order to enter or leave the chamber. This compartment is purged each time the outer door is opened.

The procedure for sealing with this equipment is as follows: The package and cover are placed on the pedestal provided. The pedestal then moves forward, causing the cover to make contact

6.3 (Cont.) ASSEMBLY PROCESSES

as it passes under the two welding electrodes. The electrodes create a continuous weld between the cover and package along two opposite sides. The pedestal travels beyond the electrodes and when it reaches the end of its travel, automatically turns 90° then travels back again. On the return cycle the electrodes weld the other two sides of the cover.

The distance between electrodes can be adjusted separately for each of the forward and reverse welding cycles. This accommodates any rectangular shaped package. Round packages can be accommodated by another fixture, the pedestal of which revolves about its own center, thereby causing the electrodes to pass along the circumference of the round package. With the power turned low and by placing a solder preform between cover and package, the process becomes a solder-sealing operation instead of weld-sealing. 80-20 gold-tin preforms are commonly used for such soldering.

1st Gross Leak Test. The leak test immediately following the sealing operation is to detect any large leaks that cannot be tolerated in the subsequent temperature tests. Other leak tests will be performed after environmental stresses because those stresses might cause leaks. In one method of gross-leak testing the sealed packages are placed in a pressure vessel which is then evacuated to a low pressure for a half hour. Then without breaking the vacuum, fluorocarbon fluid is let into the vessel so that the parts are submerged. Then the vacuum is changed to a pressure of 30 psig minimum.

This pressure is intended to force the fluorocarbon through any leaks in the package seal. The pressure is maintained for two hours.

5.2 (Cont.) ASSEMBLY PROCESSES

The package is then removed from the pressure container and submerged into another liquid fluorocarbon at 125°C with ambient pressure. Because the boiling temperature of the first liquid is 55°C, any liquid inside the package will begin to boil when placed in the second liquid. The boiling liquid creates pressure inside the package and the pressure forces liquid and gas out through leaks in the seal. These escaping fluids form bubbles that indicate the presence of the leak.

Another method of gross leak testing subjects the parts to a vacuum then a liquid dye is introduced into the chamber. Pressure is then applied to force the dye into any openings. After several hours under pressure, the parts are removed and all the dye is cleaned from the outside. The parts are inspected under magnification to insure all dye has been removed. The parts are then placed in a vacuum which draws out any dye that had previously penetrated into the part. Inspection is then done under magnification to determine the presence of any dye, which is the indication of a leak.

Parts that fail the gross leak test are degreased then vacuum baked for 24 hours at 125°C before being recycled to the cover sealing process.

Environmental Screening. High reliability hybrids are subjected to several environmental stresses. Requirements vary widely, but the most common stresses are temperature cycling, temperature shock, constant acceleration, and mechanical shock and vibration.

Temperature cycling subjects the hybrid to several cycles of from high to low temperatures, with 5 minutes maximum transition time

6.3 (Cont.) ASSEMBLY PROCESSES

between each extreme. Ten cycles from -55 to $+125^{\circ}\text{C}$ is common. This cycling is typically performed by transferring the parts from one chamber to another, each of which have been preset to the high and low temperatures.

Temperature shock means subjecting the hybrid to several cycles of immediate change from high to low temperatures. The hybrid is removed from liquid at 125°C then immersed in liquid at -55°C with a maximum of 10 seconds elapsing between. The part remains for five minutes in each liquid. 10 to 15 cycles of this test are typical.

In the constant acceleration test the hybrid is placed inside a centrifuge and usually oriented so that the centripetal force exerted by spinning will tend to pull the components vertically off the substrate. (Y_1 axis.) (Sometimes other orientations are also specified.) 5,000 to 30,000 G forces for one minute are the most frequently specified.

Mechanical shock is exerted by mounting the hybrid on a metal block then dropping that block onto a material whose shape and composition dictate the impact on the block. Typical is five shocks of 1,500 G, lasting 0.5 milliseconds, applied in each of three mutually perpendicular axes.

The hybrid is typically vibrated on a shake table whose frequency and amplitude can be controlled. The typical requirement is 20 G peak or 60 cycles per second, with 0.06 inch total excursion. The frequency is varied from 20 to 2,000 Hz. The entire frequency range is applied 4 times in 3 mutually perpendicular directions. A total of 48 minutes is the minimum requirement.

6.3 (Cont.) ASSEMBLY PROCESSES

2nd Electrical Test. Because all parameter tests will be repeated later, it is typical that after environmental screening a simple test is performed. It is sufficient at this point to demonstrate that all the components are functioning and are properly connected. Failures at this point can be recycled to have welded covers ground off and soldered or epoxied covers removed with heat.

Burn-In. This test puts a dummy load on the hybrid then runs the hybrid at its high power level continuously for 168 hours (7 days). The test is sometimes performed at the high ambient temperature of the specification. (100°C is commonly required.)

Fine Leak Test. This test for small leaks cannot detect large leaks, so a gross leak test should follow this one. Fine leaks should be tested before gross leaks because the materials used for gross leak testing might temporarily close a small hole, causing it to go undetected.

Several methods are acceptable to high reliability specifications. One involves the package being subjected to radioactive gas under pressure then removing the package and subjecting it to vacuum. Any gas that had been forced into the package can be detected as it is drawn out by the vacuum. This procedure can detect both fine and gross leaks by measuring the amount of radioactive material introduced into the hybrid.

The same basic procedure can be followed using helium. In some cases helium is sealed into the package during the original cover sealing process. When such a package is subjected to vacuum, the helium can be detected if it escapes through an opening.

6.3 (Cont.) ASSEMBLY PROCESSES

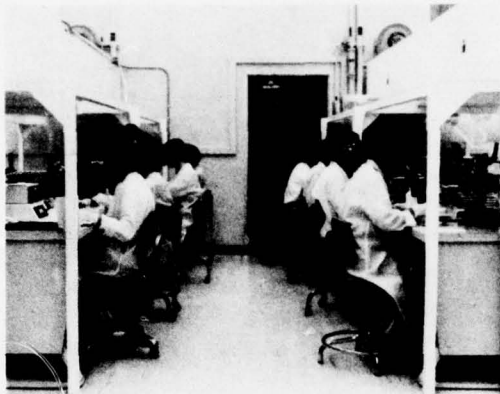
2nd Gross Leak Test. This is a repeat of the previously described gross leak test.

Final Electrical Test. This test checks the electrical function of the hybrid to all the parameters of the specification.

Failures at this point can have the covers removed and the defects reworked only if the maximum allowable rework cycles have not been done. The decision to rework failures is often based on whether it is more cost effective to rework or to originally have produced more than the required quantity.

Final Inspection. This last inspection prior to shipping the hybrid checks for cleanliness of the hybrid and verifies that the markings have not been disturbed. Also this step verifies that all previous required steps have been accomplished. It is at this point that the operations traveler document (which has accompanied the part throughout the assembly sequence and now records the history of the part) is "signed off" and filed.

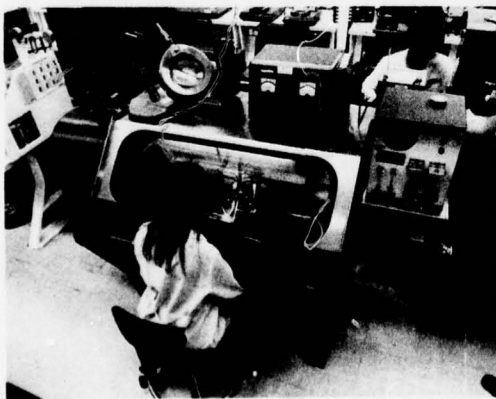
6.3 (Cont.) ASSEMBLY PROCESSES



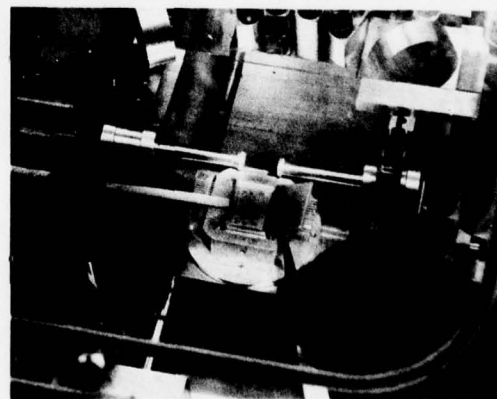
OPERATORS WORKING AT
LAMINAR-FLOW CLEAN BENCHES



WIRE BONDING



COVER-SEAL CHAMBER



WELDING ELECTRODES INSIDE
COVER-SEAL CHAMBER

SECTION 7 LAYOUT DESIGN

All of the hybrid engineering and manufacturing considerations mentioned in previous sections are brought to bear in creating the hybrid design layout. The specific groundrules and general guidelines shown in this section are preceded by text that explains the reasons for them. Some of this text reiterates information given in previous sections, in order that this section may be more independently comprehensive.

The only reason for creating any electronic product is that the product perform its electronic function. The layout guidelines and groundrules presented herein all presume that there is no tradeoff within the electrical performance requirements. Instead, the tradeoffs referred to are those that make hybrids easier to build, readily testable, more easily repairable, and electrically reliable.

The groundrules are typically stated as "preferred" and "minimum" requirements. When the design cannot meet the preferred requirements and must be established between the preferred and the minimum, decisions must be made that involve tradeoffs between one groundrule and another.

The layout design guidelines will repeatedly call attention to the fact that making optimal tradeoffs requires knowledge of the electrical requirements and of the processes and equipment that will be used in the manufacturing and testing.

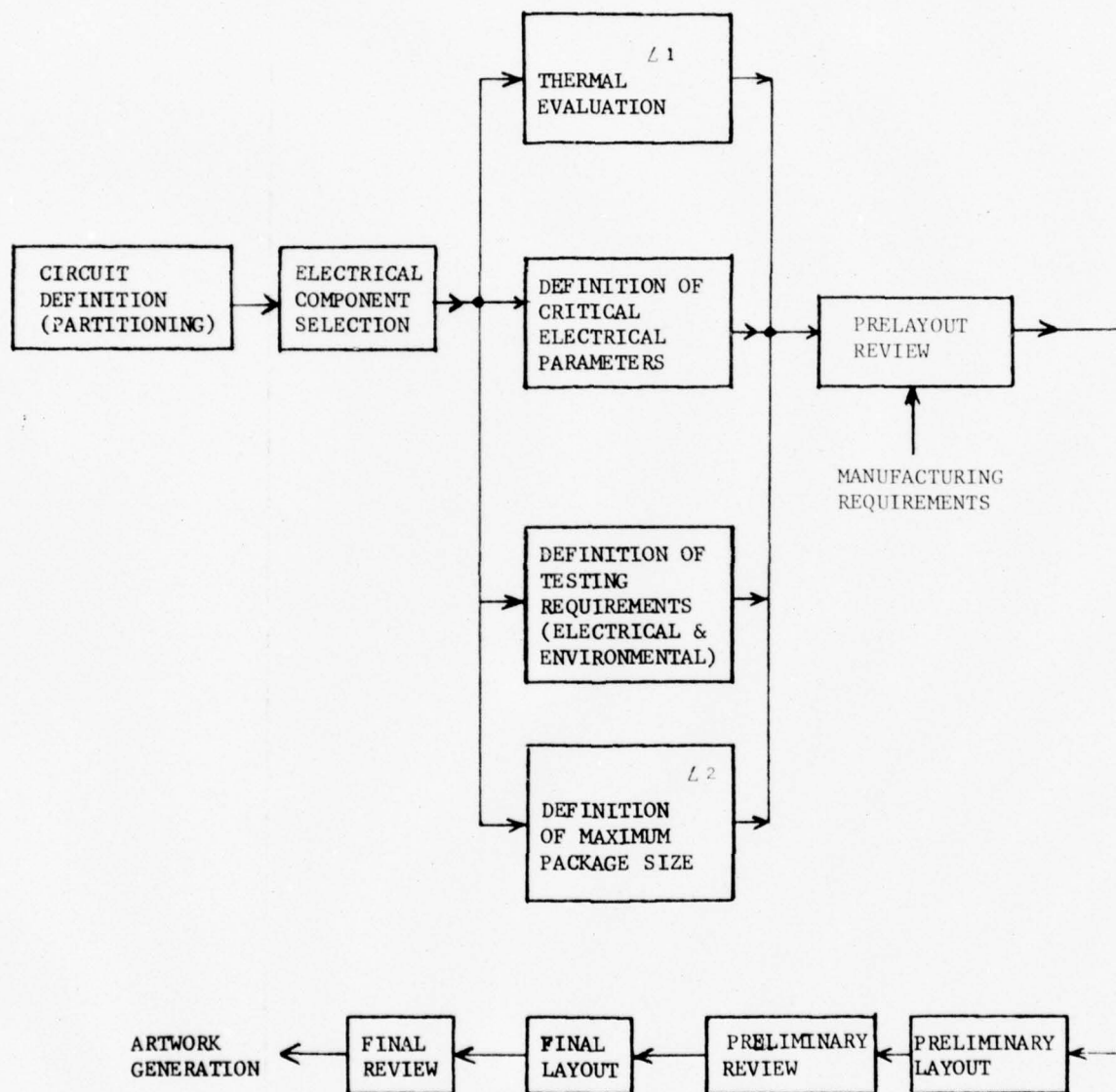
7.1 GENERAL DESIGN CONSIDERATIONS

More is required of a design layout than that it simply meet the interconnections described on the electrical schematic. Figure 7.1-1 graphically depicts the sequence of activities usually required to generate a final design layout. These activities are the engineering considerations to be accomplished either by design groups or by individual designers.

The first engineering activity related to a specific hybrid is the defining of the electrical circuit for that hybrid. This definition usually comes as a result of the partitioning of the total system circuit into smaller units. Although this partitioning function is done at the systems engineering level, layout designers often participate in the defining of the hybrids. The primary layout considerations are: how much can be, and how much should be, put into a specific hybrid.

It is typically the layout designer's function to design the resistors that are to be fabricated as an integral part of the substrate. However, it is not unusual that the selection of some purchased components is left to the layout designer. He chooses those that best suit his layout size. This is permissible only when the schedule includes enough time to permit a delay in purchasing these components. The designer should make selections from a minimum variety of parts, in order to minimize the stocking requirement and to gain a price advantage by buying large quantities and few varieties. The philosophy of basing a design on the minimum variety of parts is applicable to all parts and should guide the selection of hybrid packages and substrates.

7.1 (Cont.) GENERAL DESIGN CONSIDERATIONS



L1 Thermal evaluation is sometimes performed as part of the layout design.

L2 This function is usually required when the hybrid is part of a larger system.

Figure 7.1-1 ACTIVITIES RELATING TO A HYBRID DESIGN

7.1 (Cont.) GENERAL DESIGN CONSIDERATIONS

The layout designer does not define critical electrical parameters, but he must obtain them from the circuit designer before starting the layout. These are the most important constraints the layout must meet. If the hybrid doesn't perform its electrical function, any other feature is insignificant.

The layout designer is often assigned the task of making a thermal evaluation as part of his design activity. A final evaluation cannot be made until after the proximity of the components has been determined, and this cannot be done until at least a preliminary layout has been generated. But even before beginning a layout, an evaluation should be made of the total wattage dissipation in relation to the total package size. The individual component dissipations should be obtained before the layout starts so that these dissipations can be considered while the design is being done. Section 3 can be of assistance in the thermal evaluation; it should be noted, however, that the information in Section 3 is elementary. If the evaluation, using Section 3, reveals a marginal design, consult an expert.

It is rarely the case that there is no maximum limit imposed upon the size of a hybrid. The maximum size is most often dictated by its place within a larger system. For whatever reason the limit is imposed, it is only the maximum that is dictated. It is always worth considering whether a smaller-size package might be sufficient. However, a word of caution is appropriate. The designer should be sure that constricting the hybrid to the smallest possible size will not create a package of extreme density that is difficult to produce and test, or that is unreliable. The information in Section 1.8 (Packaging Density) provides a yardstick by which the package size can be evaluated.

7.1 (Cont.) GENERAL DESIGN CONSIDERATIONS

Multilayer substrates require continuity testing. If a universal probe fixture is to be used, all probe points must be in pre-determined locations. (See Sections 4.3 and 9.9). Electrical testing often involves probing inside the hybrid to isolate certain signals. The hybrid should have adequate space around any point where a probe might need to be placed. This is particularly important in a hybrid because the exposed components and very small wires can be damaged very easily. Environmental test requirements can also place unusual constraints upon the design. Stringent temperature environments can influence the thermal evaluation. Severe shock or vibration requirements may dictate the need to keep all wires unusually short.

In summary, if the prelayout review shown in Figure 7.1-1 is not conducted as a formal group meeting, it nevertheless behooves the layout designer to personally assure himself that he has all pertinent information before proceeding with the design.

7.2 PRELAYOUT REVIEW

Prior to beginning the actual layout, the designer should have, as a minimum, the answers to the following questions:

- o Is the electrical circuit exactly as defined? Are any changes anticipated?
- o Are all electrical constraints clearly understood?
- o Which components may be mounted outside the hybrid package if it becomes necessary?
- o Can the thermal requirements be met? Does the thermal evaluation indicate a marginal condition?
- o Is the electrical component parts list complete? (Including which resistors will be integral with the substrate?)

7.2 (Cont.) PRELAYOUT REVIEW

- o Is there a maximum limit to the package size?
- o Must the package be chosen from a list of predetermined standards?
- o If the package has been selected, does it appear to be adequate? Can its size be reduced?
- o Are all testing requirements clearly understood (both electrical and environmental)? Do these place any unusual constraints upon the design.
- o Must the manufacturing materials be totally nonorganic?
- o Which manufacturing processes are available?
- o What equipment is available for manufacturing?
- o Will the substrate be fabricated as thick or thin film?
- o What equipment is available for testing? If multilayers are required, will the substrate checkout be manual or automatic?
- o Are there any requirements not mentioned in this list?
- o After considering all the above, is there a definite priority^{L1} applicable to the design groundrules?

7.3 UNIVERSAL LAYOUT GUIDELINES

The following guidelines should be considered for any layout design.

- o The layout should be treated as an engineering document, even though it is not usually part of the official drawing package used for fabrication. It should contain as a minimum: title, document number, approval signatures, and provisions for revisions. Revision status should be indicated on the layout along with the date of revision.
- o 20X scale is preferred. It is most commonly used.
- o Preferably, the layout should be on mylar. Mylar is more stable than vellum or paper. The layout is more accurate.
- o Layout lines should lie on a grid pattern wherever feasible. 10-to-the-inch or 20-to-the-inch grids are recommended.

^{L1} "Priority" is to be interpreted as the order of importance of the various design groundrules.

7.3 (Cont.) UNIVERSAL LAYOUT GUIDELINES

- o All layout lines should be drawn on the grid lines or on half grid location. (Any line drawn between two grid lines is understood to be half-way between the two grids.)
- o Any layout line that cannot be on grid or half-grid must be dimensioned to clarify its exact position.
- o If the layout is drawn directly on a mylar grid, the grid will then always remain with the layout.
 - a. Black-line grid will appear on a print of the layout. This may sometimes be desirable. However, layout pencil lines may be difficult to distinguish from black grid lines.
 - b. The blue-line grid does not appear on a print of the layout.
 - c. A dot-pattern mylar grid is most desirable. (The dots are only at the points that would have been the intersection points of grid lines.) A black dot pattern will appear on a print of the layout, and will not obscure the layout pencil lines.
- o If plain mylar without preprinted grid is used, it should be placed over a mylar grid while the layout is being done. Two alignment points of the grid should be shown on the layout in order to realign after layout is removed from the grid.
- o If the artwork is to be generated by cutting film with a coordinatograph, then having only horizontal and vertical lines is a great advantage. If the artwork is to be manually taped, then horizontal and vertical lines are still desirable, but the advantage is not as great.
- o If diagonal lines are needed, 45° is preferred. Angles that can be defined by any two grid points are next in priority. Angles that cannot be defined as two grid points should be dimensioned on the layout.
- o The corners (intersection of two lines) should be sharp, not radiused.
- o Use special cross-hatch or color code to indicate all thick film resistors that will be fabricated from the same paste. This facilitates artwork generation.

7.3 (Cont.) UNIVERSAL LAYOUT GUIDELINES

- o Use of the color red on the layout needs special attention because red cannot be seen when red rubylith is placed over it. This fact can be used to advantage.
 - a. When the artwork patterns are being generated, it can be a distraction to have other lines appearing on the layout.
 - b. If red color is used to draw component outlines and wiring, it will fade out under the red artwork film. This fade-out leaves only the layout lines that define the actual artwork appearing while the artwork is being cut on a coordinatograph.
- o Standardize all coding (colors and symbols).
- o Package pin numbers should be assigned in counter-clockwise order, as the layout is viewed looking down on the package. The sequence should start in one corner of the package.
- o Wherever feasible, enlarge conductor tracks to form pads for bonding wires from substrate to package leads.
- o It is recommended that two wires be used from package leads to substrate bonding pads, wherever high current or low ohmic requirements exist. Such double wire bonds also increase reliability.
- o On the layout, the signal name for each package pin should be shown.
- o Where space permits, indicate on the layout the electrical function of each I.C. chip terminal for more effective layout evaluation and for electrical checkout. Where space is limited, show the I.C. terminal number.
- o The substrate and package size should be called out on the layout.
- o It is desirable to place a symbol in the substrate artwork in order to indicate the substrate orientation to the package. Pin No. 1 is usually chosen as the place for the symbol.
- o Indicate whether the backside of the substrate is to be metallized. The exact dimensions of the backside metallization should be indicated.
- o The size and material of all bonding wires should be indicated on the layout. Symbols can be used to distinguish the differences.

7.3 (Cont.) UNIVERSAL LAYOUT GUIDELINES

- o Whenever more than one artwork pattern is required for one substrate, there should be marks (or targets) on each artwork to provide for aligning them with each other.
- o The layout should have notes that contain, as a minimum:
 - a. A cross-reference to the applicable schematic, including the appropriate schematic revision status.
 - b. An explanation of all symbols and color coding used on the drawing.
 - c. A callout of the substrate and package materials.
 - d. The method of package sealing.
 - e. The method of attachment of all components, including that of the substrate to the package.
 - f. The identity of all high-wattage components, and the wattage dissipation of each.
 - g. For thin-film integral resistors, the ohms-per-square resistivity of the resistor material.
 - h. For all integral resistors, dimensions should be shown when the edges do not lie on grid.
 - i. For thick-film integral resistors, the various resistive pastes should be cross-referenced to the appropriate resistors. The resistor dimensions should also be shown. (A chart is suggested for efficiency.)

7.4 PRELIMINARY LAYOUT

In the majority of cases, it is advisable to create some form of preliminary layout.

In any individual design, the question of whether a preliminary layout will be necessary is a matter of the designer's judgment. The best judgment is, of course, based on experience; but as a generalization, those designs that fall in the high-density category merit a preliminary layout.

An important consideration in favor of a preliminary layout is that less-than-optimal designs often result when a final configuration is drawn before a preliminary overall view has been evaluated. These less-than-optimal designs occur as a result of the following sequence:

1. Eliminating a preliminary layout means that the designer's intention is to make the "first pass" suffice as the final configuration. He then must, from the beginning, expend the time and effort to make that first pass dimensionally accurate.
2. Since he cannot exactly predict the space required, he designs to minimum guidelines.
3. By the time the layout is completed, the designer is psychologically committed to that configuration on which he has expended "so much" energy.
4. Any excess space will only be seen after the designer has committed himself (i.e., after the layout is completed).
5. At this point in the sequence, no one (neither the designer nor the supervisor) wants to expend additional time or effort to completely redraw and respace the entire layout. (especially since it is such a temptation to rationalize that "it meets the guidelines").
6. The end result is a layout that meets only the minimum requirements but could have been improved to better than minimum.

7.4 (Cont.) PRELIMINARY LAYOUT

The minimal objective in a preliminary layout is to translate the symbolic electrical schematic into a complete overall physical picture as soon as possible and to expend the least effort necessary to achieve that physical picture.

In the preparation of a preliminary layout, a variety of abbreviated graphic techniques can be used to save time and help avoid a premature commitment. The following groundrules are sufficient for a minimal preliminary layout.

- o Free-hand drawing (without straight-edge) is adequate.
- o It is not critical that components be drawn to exact size. An approximation of size is helpful, but not mandatory.
- o Draw conductors as single-width pencil lines.
- o Show voltage and ground lines as wider lines, simply as a reminder; not mandatory.
- o As preliminary layout proceeds, maintain excess space between components and between conductor lines in order to make changes easily.
- o A good approximation of the actual space requirements can be determined mathematically by adding up the real sizes of the components and the conductor tracks.
- o To distinguish bonding wires from conductor tracks, color can be used.
- o Show all chip bonding pads in their positions relative to the corners of the chip (i.e., draw each pad at the edge of the chip where it truly appears, but the exact spacing along that edge is not critical).
- o Package pins can usually be determined at the preliminary stage.

Note: preferred package pin numbering is counterclockwise.

7.4 (Cont.) PRELIMINARY LAYOUT

Figure 7.4-1 is an example of such a minimal preliminary layout for a single-layer substrate.

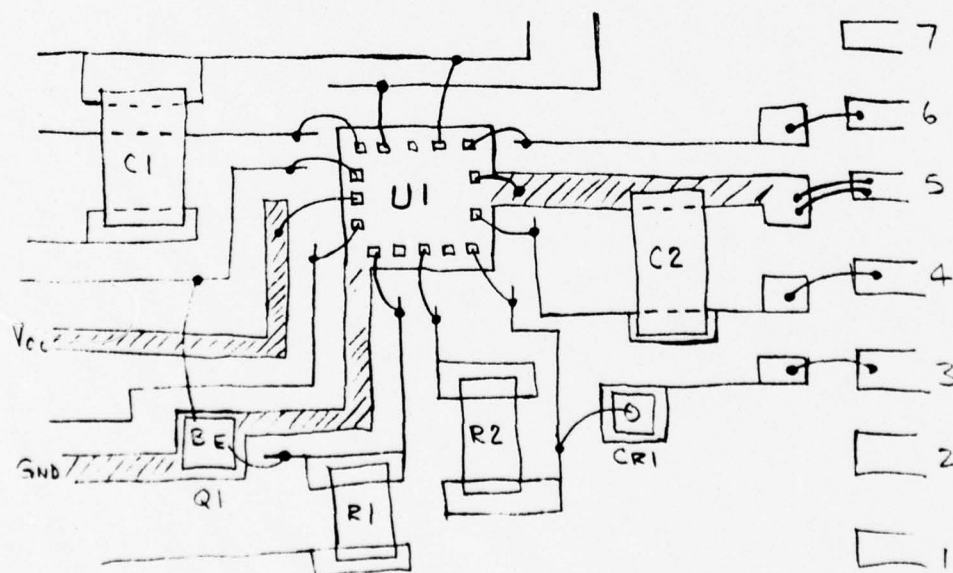


Figure 7.4-1 EXAMPLE OF MINIMAL PRELIMINARY LAYOUT (SINGLE LAYER)

7.4 (Cont.) PRELIMINARY LAYOUT

Although the type of layout shown (Figure 7.4-1) does serve the minimal purpose of creating a physical picture, it obviously could have been more definitive. The next example depicts a preliminary layout technique that is more definitive, and requires somewhat more accuracy.

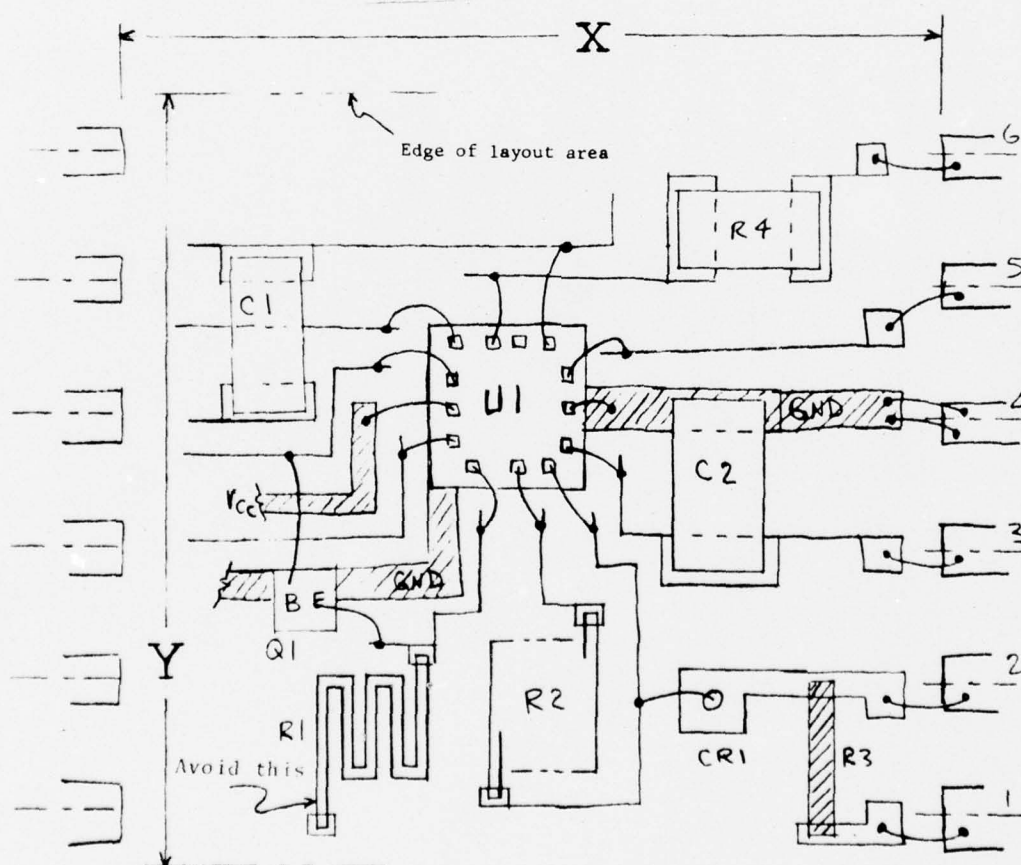


Figure 7.4-2 EXAMPLE OF SEMIACCURATE PRELIMINARY LAYOUT (SINGLE LAYER)

7.4 (Cont.) PRELIMINARY LAYOUT

The following groundrules are sufficient for such a semiaccurate preliminary layout.

- o All components and package pin spacing (E to E only) should be drawn to correct size.
- o 20x scale is suggested.
- o Components and pin spacing need only be measured accurately one time, and drawn on a separate piece of paper to the scale selected for the layout. After once being drawn accurately, they can be traced on the preliminary layout. This includes resistors that are to be integral with the substrate.
- o The same accurate pictures can later be traced on the final layout.
- o When each component is traced on the preliminary layout, its mounting pads should be included (see Section 7.6).
- o Although the accurate picture done on separate paper should be drawn with a straight edge, free-hand tracing (without straight edge) is adequate for the preliminary layout, as long as the corners are drawn to accurately define the outermost dimension of the object traced.
- o Allow excess space between components and conductor lines in order to make changes easily. The actual space required for conductor tracks can be determined mathematically.
- o The overall size shown as dimensions X and Y in Figure 7.4.2 need not be accurate in preliminary layout. When preliminary layout is complete, the mathematical sum of the sizes of mounting pads, lines and spaces will indicate the overall size.
- o R1 is an example of what not to do. Complete delineation of a serpentine resistor is unnecessary.
- o R2 is an adequate abbreviated outline of a serpentine resistor. Note: The overall size should be accurate.
- o R3 is integral with the substrate. It is shaded only to distinguish it from R4, which is a chip resistor.

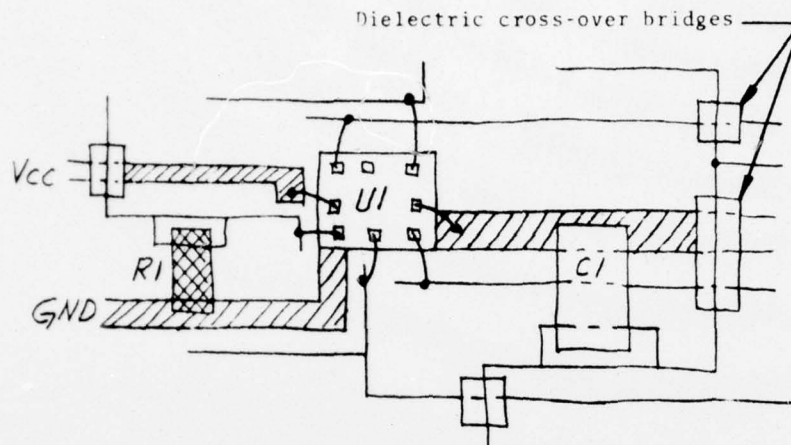
7.4 (Cont.) PRELIMINARY LAYOUT

- o Any resistor that is integral with the substrate may need to have its shape modified during final layout in order to best utilize available space. (Of course, its resistance value must remain unchanged. See Section 7.8.)

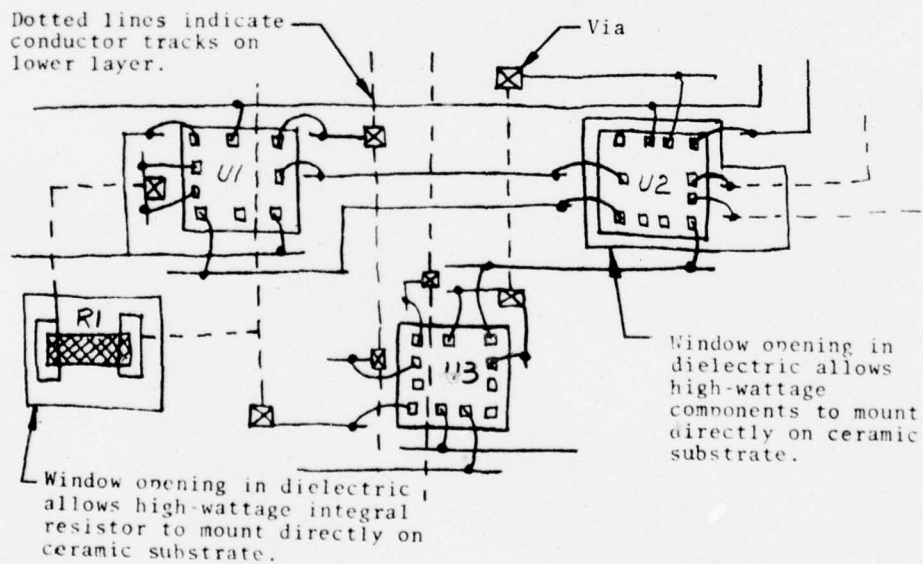
The advantage of this semiaccurate preliminary layout (Figure 7.4-2) over the previously shown minimal configuration (Figure 7.4-1) is that 7.4-2 is much more definitive. While it does require additional effort, that effort during preliminary layout reduces effort during the final layout. Figure 7.4-2 is much closer to the final configuration than Figure 7.4-1.

Each of the previous examples was a single layer design. Abbreviated drafting techniques can also be used for multilayer designs. Figure 7.4-3 shows examples of preliminary layouts for multilayer designs using dielectric cross-over bridges and using continuous dielectric layers. (When more than two layers are required, the layout may be clearer if two sheets are used. Each sheet can depict two layers.)

7.4 (Cont.) PRELIMINARY LAYOUT



LAYOUT FOR DIELECTRIC CROSS-OVER BRIDGES



LAYOUT FOR CONTINUOUS DIELECTRIC LAYERS

- o Color coding can be used to indicate conductor tracks on different layers.
- o When dielectric is a continuous layer, its outline need not be drawn.

Figure 7.4-3 EXAMPLES OF PRELIMINARY MULTILAYER LAYOUT

7.5 CONDUCTOR AND RESISTOR LINES AND SPACING

In the preparation of a hybrid microcircuit layout, some of the first groundrules to be established are the minimum and preferred dimensions for conductors and resistors and the spaces between them. In this section, the minimums referred to are the limits of manufacturing capability. Other design constraints often dictate that the dimensions must be larger than the manufacturing minimums (e.g., constraints pertaining to high current, ground reference, thermal dissipation, wire bonding, etc.).

The criteria for thin and thick film designs are different due to the processes involved in the fabrication. Within the thick film category there are unique requirements for multilayer technology.

7.5.1 Thin Film Lines and Spaces

The preferred width is 5 mils (0.127 mm) for conductors. These dimensions will provide high fabrication yields when either of the two common thin film processes are used (i.e., panel plating or pattern plating).

As a generalization, 2 mils is considered a workable minimum that still has the potential for good yields. The word "potential" as used here means that the yields will be high if all the process variables can be maintained within a narrow range.

Layouts are typically drawn so that pencil lines lie on a grid pattern 100 mils (2.54 mm) x 100 mils or 50 mils (1.27 mm) x 50 mils. For drafting convenience, 2.5 mils (0.063 mm) is frequently used as the minimum, since it allows the continuation of the full-grid or half-grid increment (2.5 mils at 20x scale measure 50 mils).

7.5.1 (Cont.) Thin Film Lines and Spaces

The absolute minimum dimensions are difficult to define. Various combinations of materials, equipment, and techniques have been utilized to achieve lines and spaces of less than 0.5 mils (0.0127 mm). These cases typically involve small quantities, and much lower fabrication yields must be accepted.

The dimensions for the spaces between adjacent conductors are the same as for the conductors themselves: preferred, 5 mils; workable minimum, 2 mils; for drafting convenience, 2.5 mils; absolute minimum, less than 0.5 mils.

NOTE: Tolerance on the substrate size should be taken into account when determining any minimum edge distance.

The distance from the edge of the substrate to the nearest conductor is preferably 7.5 mils (0.190 mm), with a minimum of 5 mils (0.127 mm). These dimensions apply to substrates that are precut to size. Thin film substrates are often fabricated as a multiple pattern on one oversize substrate, that is later broken into smaller substrates. (See description of scribe and break.) Additional space is desirable to permit a tolerance on the location of the scribe lines, and the broken substrate edges may also be more ragged. For these reasons, the edge distances for "scribe and break" substrates are: preferred, 10 mils (0.254 mm); minimum, 7.5 mils.

Thin film resistors can be produced with high yields when the width is 5 mils (0.127 mm). The generally accepted minimum is 2.5 mils (0.063 mm). The absolute minimum can be less than 1.0 mil (0.0254 mm).

7.5.1 (Cont.) Thin Film Lines and Spaces

NOTE: The above resistor dimensions apply to the resistor in areas other than the trim bar (see Sections 6.1 and 7.8 for trimming information). In the area of the trim bar a 10-mil (0.254 mm) width is preferred, with a minimum of 7.5 mils (0.190 mm).

Reminder: The resistor's electrical and thermal requirements usually dictate its geometry more than the fabrication limitations. See Section 7.8 for resistor design guidelines.

The space between resistors is 5 mils (0.127 mm) preferred; 2 mils minimum; for drafting convenience 2.5 mils (0.063 mm); absolute minimum less than 1.0 mil (0.0254 mm).

Because the resistors and conductors are on separate masks, the distance between resistors and conductors should be larger to allow for misalignment between the two masks. The preferred space is 7.5 mils (0.190 mm); the minimum is 5 mils. These dimensions apply in areas other than adjacent to the resistor trim bar. The space required adjacent the trim bar is 10 mils (0.254 mm); minimum 7.5 mils (0.190 mm).

The configuration recommended for a conductor/resistor interface using pattern-plating processing is different from one using panel-plating processing. For pattern plating, the conductor should be 5 mils (0.127 mm) wider on each side of the resistor; the conductor and resistor should overlap 5 mils; and the conductor should extend 5 mils beyond the overlap. For panel plating, the conductor width should be equal to the resistor (no overlap is required) and the conductor should extend 10 mils (0.254 mm) beyond the end of the resistor before a change of conductor direction. These dimensions for the two distinct interface

7.5.1 (Cont.) Thin Film Lines and Spaces

configurations permit easy alignment of the respective resistor mask to the conductor pattern. (See Section 6.1 for a description of the processes.) These differences in pattern plating versus panel plating emphasize the designer's need to know about which technique will be used.

In thin film technology, both conductors and resistors are fabricated by selective acid etching of the film materials. The etching undercut factor is one of the important processing variables. Since the amount of undercut is affected by the material thickness through which the acid must etch, the net result is that absolute minimum line widths are greatly influenced by the material thickness. This factor is an example of the interrelationship of variables.

NOTE: Since extremely small lines or spaces require unique critical processing, it is not recommended to combine both critically small and normally preferred sizes within one layout.

Any hybrid designed to the limit of any fabrication capability should be approved only after a consultation with the processing group.

Table 7.5.1-1 summarizes the minimum and preferred dimensions for thin film designs, as discussed in this section. Figures 7.5.1-1 and 7.5.1-2 illustrate the dimensions called out in Table 7.5.1-1.

7.5.1 (Cont.) Thin Film Lines and Spaces

Table 7.5.1-1 DIMENSIONS FOR THIN FILM LINES AND SPACES

TYPE OF LINE OR SPACE	MINIMUM ^{/5}		PREFERRED		SEE FIGURE
	mils	mm	mils	mm	
Conductor Width	2.0 ^{/1} ^{/4}	0.0508	5.0	0.127	7.5.1-1 (1)
Space between Adjacent Conductors	2.0 ^{/1} ^{/4}	0.0508	5.0	0.127	7.5.1-1 (2)
Conductor to Edge of Substrate: Pre-cut Substrates	5.0	0.127	7.5	0.1905	7.5.1-1 (3)
Scribe-and-Break Substrates	7.5	0.1905	10.0	0.254	
Space between Conductors and Resistors Not In Area of Trimming	5.0	0.127	7.5	0.1905	7.5.1-1 (10)
Conductor Resistor Overlap (Pattern Plating Only)	2.0 ^{/1}	0.0508	5.0	0.127	7.5.1-1 (8)
Conductor Dimension beyond Overlap (Pattern Plating Only)	2.0 ^{/1}	0.0508	5.0	0.127	7.5.1-1 (9)
Conductor Width at Resistor Interface: Panel Plating	2.0	Equal to Resistor		5.0	7.5.1-2 (12)
Pattern Plating ^{/2}					7.5.1-1 (11)
Resistor Width: Not In Area of Trimming ^{/3}	2.5 ^{/7}	0.0635	5.0	0.127	7.5.1-1 (4)
In Area of Trimming ^{/3}	10.0	0.254	12.5	0.317	7.5.1-1 (5)
Space between Resistors Not In Area of Trimming	2.5 ^{/7}	0.0635	5.0	0.127	7.5.1-1 (6) 7.5.1-2 (6)
Space required Adjacent to Resistor Trim Bar:	7.5	0.1905	10.0	0.254	7.5.1-1 (7) 7.5.1-2 (7)
Laser Trimming					
Abrasive Trimming ^{/6}	15.0	0.381	25.0	0.635	
Length of Straight Conductor beyond Resistor (Panel Plating Only)	5.0	0.127	10.0	0.254	7.5.1-2 (13)

/1 For drafting convenience 2.5 mils is often used.

/2 Dimension indicates amount conductor extends beyond each side of resistor.

/3 See Section 7.8 for resistor trimming information.

/4 Critical processing can produce less than 0.5 mil (0.0127 mm).

/5 To be used only when necessary.

/6 Abrasive trimming seldom, if ever, used for thin film resistors.

/7 Critical processes can produce less than 1.0 mil (0.0254 mm).

7.5.1 (Cont.) Thin Film Lines and Spaces

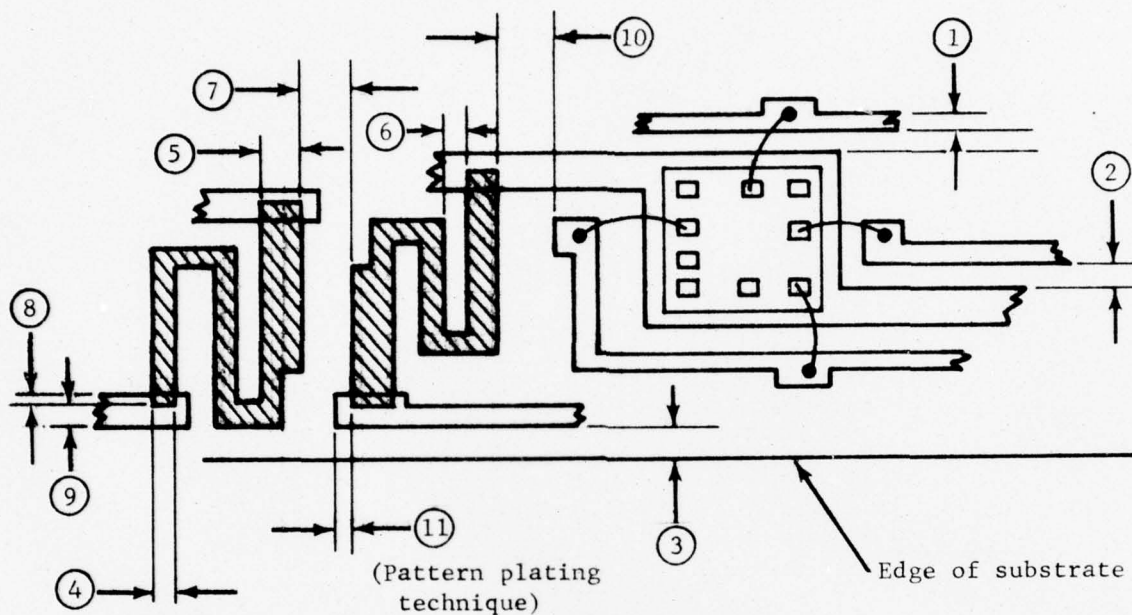
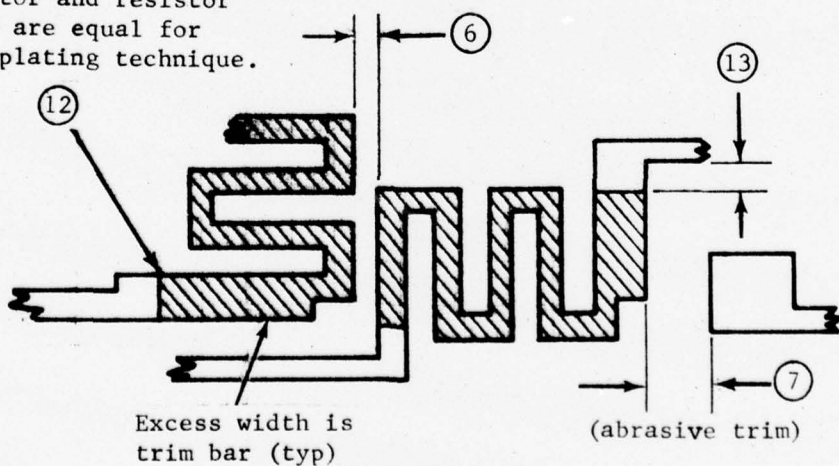


Figure 7.5.1-1 CONSTRAINTS FOR THIN FILM LINES AND SPACES

Conductor and resistor widths are equal for panel plating technique.



Note: Resistor/conductor interfaces shown here apply to panel plating only.

Figure 7.5.1-2 ADDITIONAL CONSTRAINTS FOR THIN FILM LINES AND SPACES

7.5.2 Thick Film Lines and Spaces

There is a wide range of expertise in producing thick film substrates. The continuous improvement in materials and equipment combined with new, constantly evolving techniques, is decreasing the sizes of thick film lines and spaces. This state of flux emphasizes the need for coordination between the layout designer and the thick-film manufacturing group.

It should be recognized that the dimensions given here are the recommendations based on fabrication requirements; other constraints usually have higher priorities than fabrication and therefore establish the need for larger-than-minimum sizes of lines and spaces in certain areas of the layout (i.e., electrical performance constraints, thermal constraints, and testing requirements).

In thick film processing, the pattern is applied on the ceramic substrate by a screen printing technique. Consistent screen/squeegee pressure over the entire working area is important to the production of small lines and spaces. Yet that pressure is affected by the ceramic's camber (curvature), which is in turn a function of the ceramic's size. (Substrate camber is commonly specified to be 4 mils (0.102 mm) per linear inch.) The size of the substrate, relative to the size of the printing screen, can also affect the overall pressure. This size ratio is usually only a factor for substrates larger than 2.00 in. The recommendations given in this section apply to substrates up to 2.00 in. by 2.00 in. When the substrate is larger, the design requirements should be confirmed by the manufacturing group that will produce the particular substrates.

7.5.2 (Cont.) Thick Film Lines and Spaces

Common high-yield design criteria require conductor lines and spaces of 12.5 mils (0.3175 mm). However, the minimum limit in any particular design is dependent on the capability of the manufacturing group that will fabricate the substrates. Consistent good yields have, in some cases, been achieved with dimensions of 5 mils (0.127 mm). Beam-lead mounting patterns have been produced with lines of 4 mils (0.102 mm) over short distances. On the other hand, there are manufacturing groups that achieve better yields producing multilayer configurations with 10 mil lines and spaces than producing a single layer substrate with lines and spaces less than 10 mils (0.254 mm). In cases where low-cost and high-production rates are the highest priorities, 15 mils (0.381 mm) has been established as the preferred dimension and 10 mils as the design minimum.

For thick film resistors, both the length and the width have minimum limits. One reason is that both conductor and resistor materials are applied as pastes (also called inks), and at the interface between the two a blending of the materials occurs during firing. The area of blending is only a few mils into the area of the resistor; but if those few mils are a large percentage of the total resistor length, then the effect on the resistor value is large.

It is important to note that the fabrication of resistors entails a larger number of variables than the fabrication of conductors. In addition to the large variety of materials, equipment, and techniques being used, there is a wide range of resistor performance requirements. When the resistor's performance is critical over various ranges of electrical and environmental conditions, the design of the resistor geometry should be closely coordinated

7.5.2 (Cont.) Thick Film Lines and Spaces

with the processing engineer. (See Sections 7.8 and 1.4 for performance data.)

Each separate resistor paste being applied requires a separate mask, therefore certain resistors within one substrate may be screened through separate masks. Additional space is recommended between resistors on separate masks in order to allow for registration tolerances between the masks.

For any particular design, the minimum dimensions are influenced by the quantities to be built. Anything can be built once, even if it means building a hundred to get one good one, but designs for large quantities should not force the manufacturing group to use critical process controls. The recommended dimensions are conservative in order to establish designs that permit high manufacturing yields without utilizing critical process controls.

A glaze is sometimes applied over resistors to improve their stability. The glaze is applied thorough a separate mask. The glaze should be 7.5 mils (0.190 mm) larger all around the resistor.

Table 7.5.2-1 lists the dimensional constraints for thick film lines and spaces. Figure 7.5.2-1 illustrates examples of the constraints listed in Table 7.5.2-1.

7.5.2 (Cont.) Thick Film Lines and Spaces

Table 7.5.2-1 DIMENSIONS FOR THICK FILM LINES AND SPACES

TYPE OF LINE OR SPACE	MINIMUM		PREFERRED		SEE FIGURE
	mils	mm	mils	mm	
Conductor Width	<u>/1</u>	<u>/1</u>	12.5	.3175	7.5.2-1 (1)
Space between Adjacent Conductors	<u>/1</u>	<u>/1</u>	12.5	.3175	7.5.2-1 (2)
Space between Conductor and Resistor on Untrimmed Side of Resistor	10.0	.254	15.0	.381	7.5.2-1 (13)
Conductor Width at Resistor Interface <u>/2</u>	5.0	.127	7.5	.1905	7.5.2-1 (11)
Space from Substrate Edge to Nearest Conductor	<u>/1</u>	<u>/1</u>	10.0	.254	7.5.2-1 (3)
Resistor Width	<u>/1</u>	<u>/1</u>	30.0	.762 <u>/3</u>	7.5.2-1 (4)
Resistor Length	25.0	.635 <u>/7</u>	35.0	.889 <u>/3</u> <u>/7</u>	7.5.2-1 (5)
Space between Resistors (On Untrimmed Sides of Resistors) <u>/6</u>					
Resistors within One Mask	10.0	.254	12.5	.3175	7.5.2-1 (6)
Resistors on Separate Masks <u>/4</u>	10.0	.254	15.0	.381	(7)
Overlap at Resistor/Conductor Interface <u>/6</u>	10.0	.254	15.0	.381	7.5.2-1 (10)
Conductor Dimension beyond Overlap	5.0	.127	10.0	.254	7.5.2-1 (12)
Space Adjacent to Resistor Required for Trimming					
Laser Trimming	10.0	.254	15.0	.381	7.5.2-1 (8)
Abrasive Trimming	15.0	.381	25.0	.635	(8)
Overglaze beyond Resistor Size	5.0	.127	7.5	.1905	7.5.2-1 (9)

/1 Consult manufacturing group.

/2 Dimension on each side of resistor width.

/3 Consult manufacturing group for critical performance resistors.

/4 Each paste type is applied with separate mask.

/5 All dimensions recommended for substrate sizes up to 2.00 in. (50.8 mm) x 2.00 in.
For larger sizes, consult manufacturing group.

/6 See special cases shown on Figure 7.5.2-1.

/7 High resistivity pastes ($> 1 \text{ M}\Omega/\square$) require longer lengths (see Section 1.4).

7.5.2 (Cont.) Thick Film Lines and Spaces

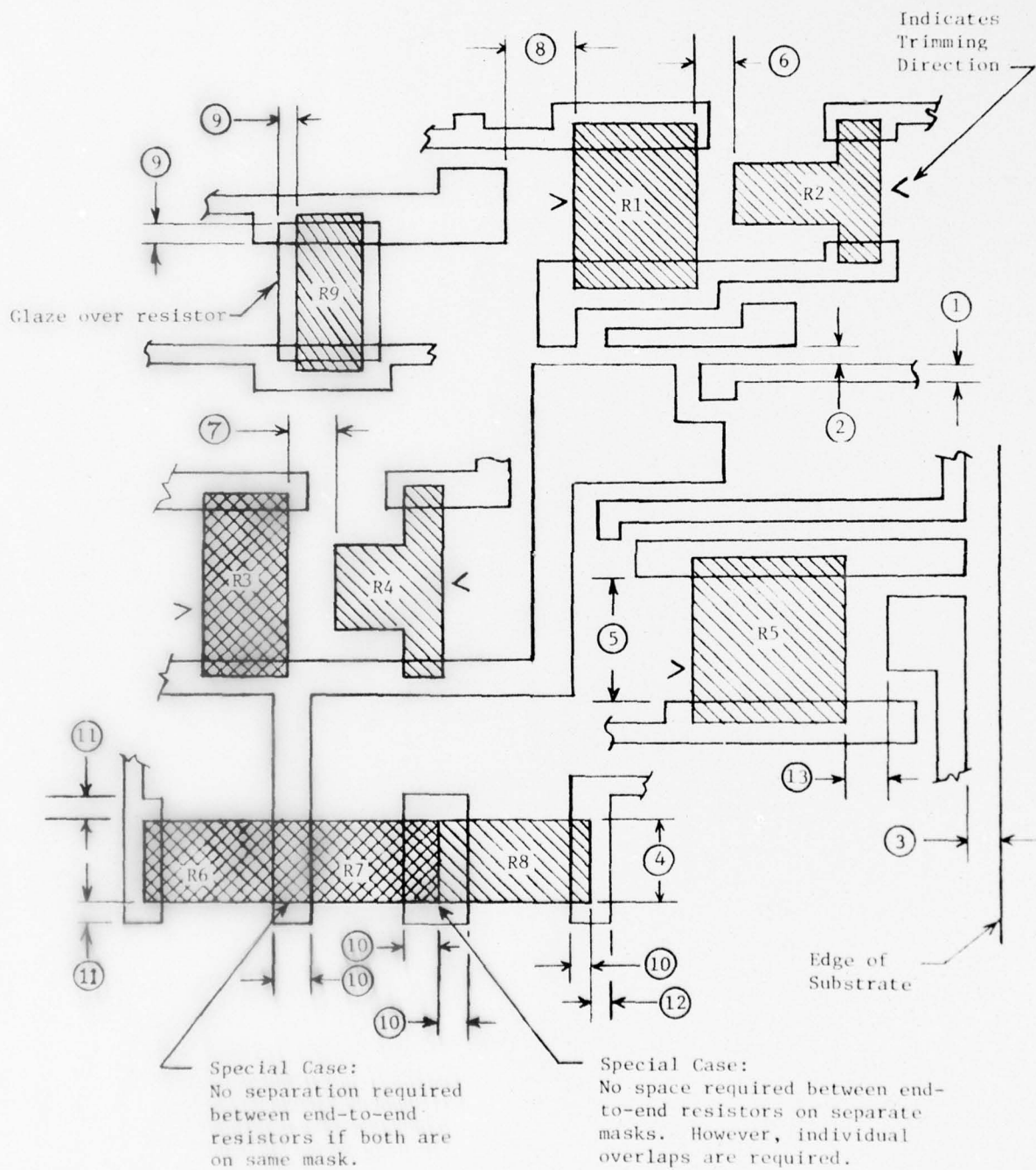


Figure 7.5.2-1 THICK FILM LINES AND SPACES

7.6 COMPONENT MOUNTING

In a hybrid microcircuit, the electronic components are typically mounted onto the surface of the substrate conductor tracks. The tracks are shaped into pads, the sizes of which are designed to accommodate the various components.

When establishing the pad sizes and spacing requirements for component mounting, the layout designer needs to take into account thermal dissipation, electrical constraints, and the materials and techniques that will be used during assembly. The recommendations given throughout this section take into account only assembly materials and techniques. Thermal and electrical requirements are discussed in other sections.

Materials and techniques used to attach components to the mounting pads vary from solder or epoxy, which creates fillets around the component to eutectic attach which adds no material around the component. Solder will typically "wet" only the metallized areas and will tend not to spread onto the bare ceramic (assuming, of course, that the amount applied is not excessive). Certain epoxies will spread indiscriminately because their viscosity becomes lower during the curing cycle.

High-reliability specifications typically prohibit the use of epoxy in the same package with semiconductors, because epoxy (or any other organic material) may have long-term, deleterious effects on semiconductors. Epoxy usage is included here, not as a recommendation, but for those instances where epoxy is not prohibited.

7.6 (Cont.) COMPONENT MOUNTING

Components can be mounted on the top surface of a multilayer substrate only if the low thermal transfer through the dielectric layers can be tolerated. Since eutectic attach of semiconductor chips requires a flat surface, the number and type of layers under the semiconductor mounting pad may need to be restricted. Compared to a continuous conductor plane, individual conductor tracks on lower layers create greater "waviness" in subsequent layers. The constraints concerning component mounting on top of multiple layers should be established by the manufacturing group.

Components can not only be mounted on the substrate, inside the package, but high-wattage components can be mounted directly on the top surface of the package base. Of course, in such a case the substrate cannot cover the entire package surface.

High-wattage semiconductor chips are sometimes premounted on gold-plated, molybdenum chips, called molytabs, prior to being installed into the hybrid. In such cases, the size of the molytab determines the mounting requirements.

On a rectangular shaped substrate, it is definitely preferred that all components be aligned parallel to the substrate edges. (A unique exception is pointed out at Q3 of Figure 7.6.1-1.

For round or odd-shaped substrates, the manufacturing group should determine the best component orientation.

This section delineates the design considerations and dimensional groundrules for mounting the various types of components commonly used in hybrid microcircuits.

7.6.1 Semiconductor Mounting

For all semiconductor chips a mounting pad 10 mils (0.254 mm) larger (all around) than the maximum size of the chip is recommended. Where eutectic attachment is intended, a smaller-sized mounting pad could suffice; but it is a better design practice to allow for the possibility that an alternative method may need to be substituted. For instance, if during assembly the eutectic equipment becomes inoperative, solder attach might be substituted. Another reason for the larger size is that if a eutectically attached chip needs to be replaced, it is not uncommon that the new chip be attached with solder or epoxy. The minimum size mounting pad is 5 mils (0.127 mm) larger (all around) than the maximum chip dimensions.

The space between a chip mounting pad and an adjacent conductor must be sufficient to prohibit the chip bonding material from shorting to the adjacent conductor. Since eutectic attach requires no additional bonding material, the standard conductor spacing can be maintained between a mounting pad and any adjacent conductor when eutectic attach is used. Where solder or epoxy is being used or planned as a rework, a 12.5 mils (0.317 mm) space is preferred. Low-viscosity epoxies require additional space, and the manufacturing group should be consulted. The minimum space should be 10 mils (0.254 mm).

Where solder or epoxy is to be used for attaching two chips on the same mounting pad, 10 mils is preferred between the adjacent chips. 5 mils is minimum.

A eutectically attached semiconductor chip (100 mils by 100 mils or smaller) should have 30 mils clearance between it and any other semiconductor chip. This large clearance is to allow for the size

7.6.1 (Cont.) Semiconductor Mounting

of the attachment tool and for the oscillating movement of the tool. Larger chips may require additional tool clearance. Also, another type of component having a greater height than a semiconductor might need to be located farther away. The manufacturing group should be consulted to determine the clearance required for the particular tool being used.

NOTE: The clearance mentioned above refers to the proximity of components; not to conductors or resistors on the surface of the substrate.

Table 7.6.1-1 lists the previously mentioned groundrules for semiconductor mounting. Figure 7.6.1-1 shows examples of the groundrules listed in Table 7.6.1-1.

Where both multilayer interconnections and high-wattage semiconductors are required on the same substrate, the chip mounting pad can be directly on the surface of the substrate and can be exposed through a window opening in the dielectric layers. If a chip is to be mounted inside such a window opening by either solder or epoxy-attach (although epoxy is not a good heat-transfer material), the space between chip and window edge should be 15 mils (0.381 mm) all around. The minimum is 10 mils (0.254 mm). Where a eutectic attach tool is to be used, the previously mentioned 30 mils (0.762 mm) clearance is needed. Figure 7.6.1-2 is a sketch of such a configuration.

7.6.1 (Cont.) Semiconductor Mounting

Table 7.6.1-1 SEMICONDUCTOR MOUNTING DIMENSIONS

MOUNTING CONFIGURATION	MINIMUM		PREFERRED		SEE FIGURE
	mils	mm	mils	mm	
Mounting Pad Dimension (All around chip) ^{L1}	5	0.127	10	0.254	7.6.1-1 (1)
Space between Mounting Pad and Adjacent Conductor:					
Eutectic-Attach ^{L2}	^{L3}		^{L3}		7.6.1-1 (2)
Solder/Epoxy-Attach ^{L4}	10	0.254	12.5	0.317	
Space between Semiconductors:					
Solder/Epoxy-Attach	5	0.127	10	0.254	7.6.1-1 (3)
Eutectic-Attach ^{L5}	^{L6}		30	0.762	7.6.1-1 (4)
Space between Semiconductor and Other Component					
Solder/Epoxy-Attach	10	0.254	20	0.508	7.6.1-1 (5)
Eutectic-Attach	^{L7}		^{L7}		7.6.1-1 (6)
Space between Semiconductor and Dielectric Window Edge:					
Solder/Epoxy-Attach	10	0.254	15	0.381	7.6.1-2
Eutectic-Attach	^{L6}		30	0.761	

^{L1} When chip is premounted on a molytab, the dimensions shown apply all around molytab.

^{L2} Wherever possible, allowance should be made for solder/epoxy substitution.

^{L3} Use standard line to line spacing to suite fabrication (either thin film, thick film or multilayer).

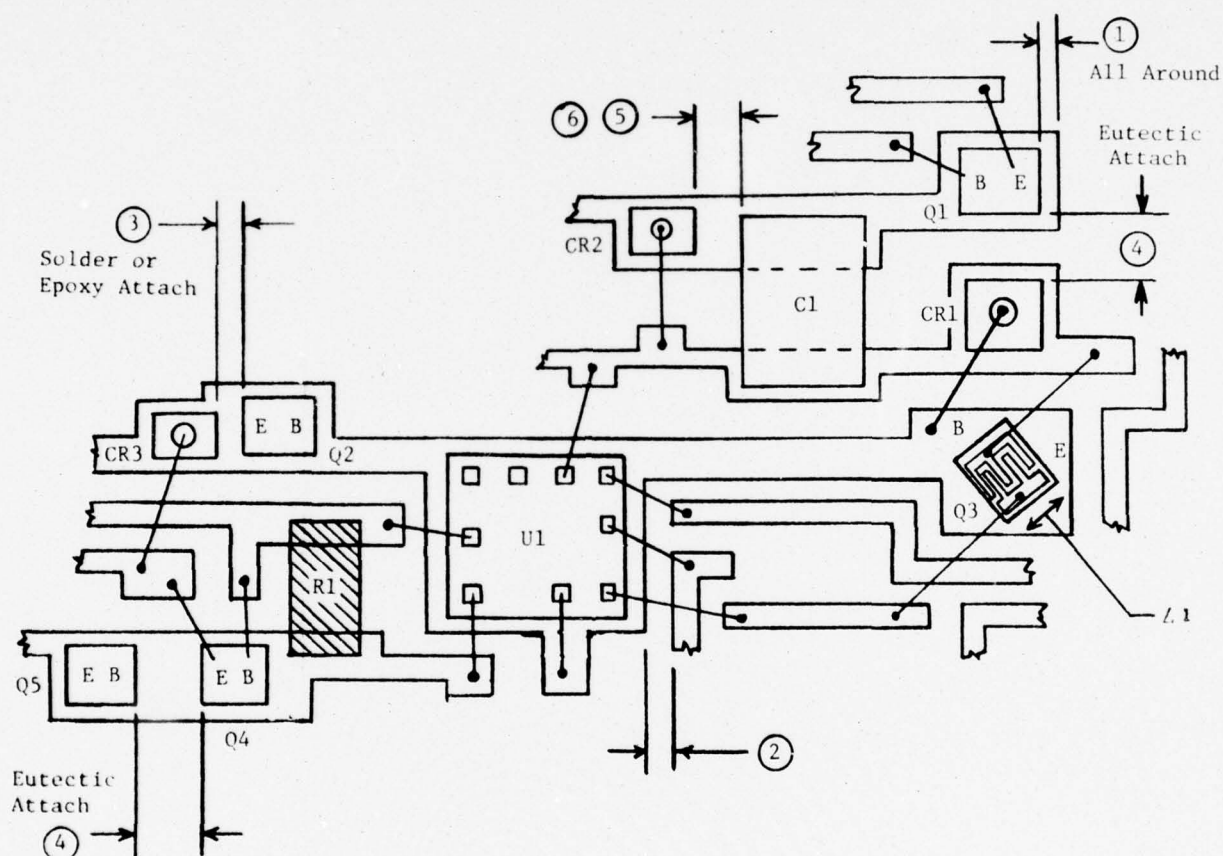
^{L4} Low viscosity epoxy may require additional space.

^{L5} For chip size up to 100 x 100 mils (2.54 mm). For larger chips consult manufacturing group.

^{L6} Consult manufacturing group.

^{L7} Space determined by height of other component and shape of eutectic-attach tool.

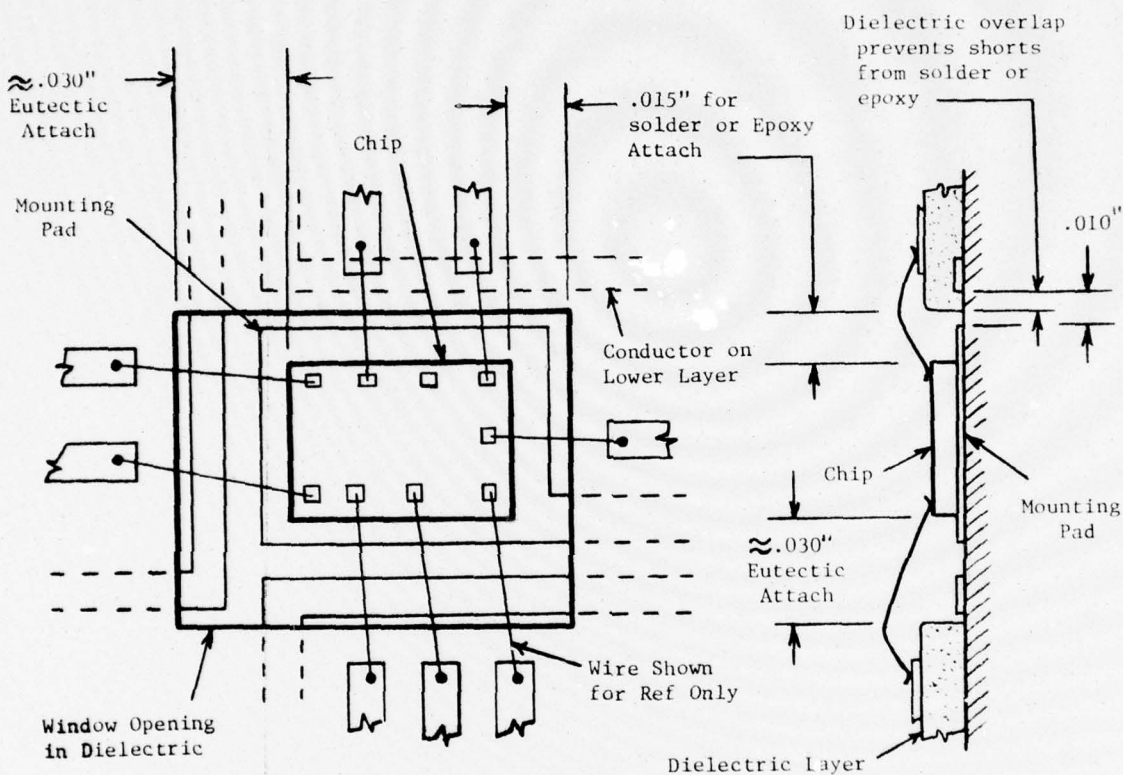
7.6.1 (Cont.) Semiconductor Mounting



L1 Bonding pads on the chip are so small, and of such a shape, that both wire bonds must be made in the direction of the arrows. In this case, the need for the wire bonds to be in a specific direction dictates that the chip be oriented diagonally. The chip mounting pad could also have been diagonal.

Figure 7.6.1-1 DIMENSIONS FOR SEMICONDUCTOR MOUNTING

7.6.1 (Cont.) Semiconductor Mounting



Note: 1. For chip sizes larger than 100 x 100 mils (2.54 mm), the eutectic-attach tool may require more clearance.

2. Dimensions shown are inches.

Metric Equivalents

in.	mm
.010	.254
.015	.381
.030	.762

Figure 7.6.1-2 SEMICONDUCTOR MOUNTING INSIDE A DIELECTRIC WINDOW OPENING

7.6.1 (Cont.) Semiconductor Mounting

Semiconductor chips can not only be mounted on the substrate but also on the surface of the package base. The clearances required are unique for any individual case. The clearances required depend on the dimensions of the package, the substrate and the attach tool.

Figure 7.6.1-3 indicates the dimensions to be considered.

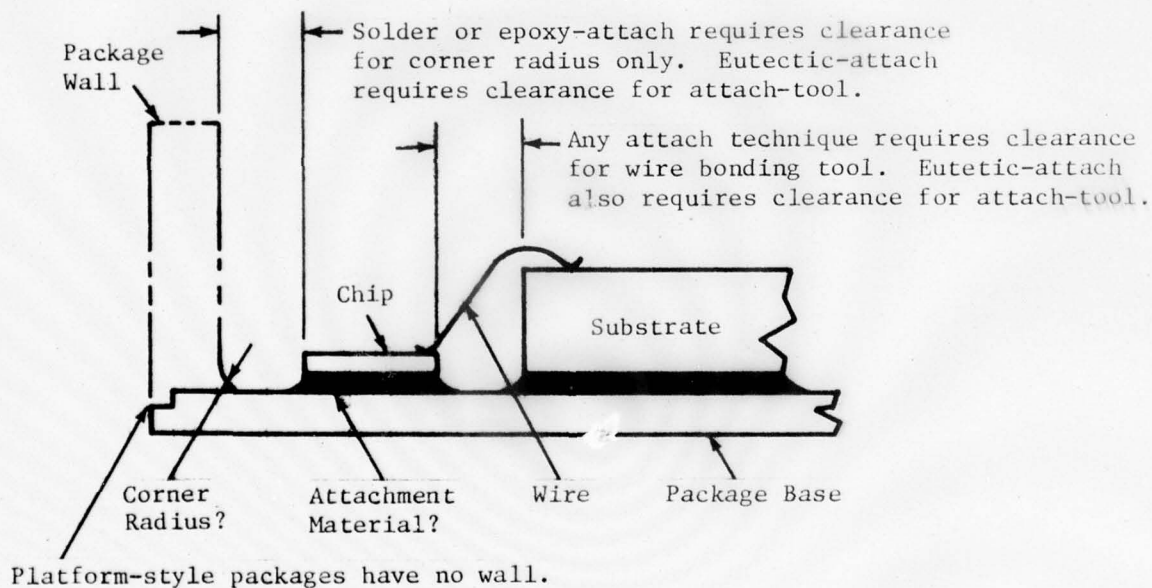


Figure 7.6.1-3 SEMICONDUCTOR MOUNTED ON PACKAGE BASE

7.6.1 (Cont.) Semiconductor Mounting

If eutectic attachment is intended, the mounting of semiconductor chips on top of multiple layers imposes unique constraints on the substrate configuration. The flatness of the mounting pad is the crucial factor. Eutectic-attach requires a flat surface. An uneven mounting pad surface will provide only three-point contact to the bottom surface of the semiconductor chip.

Where solder or epoxy attach is intended, the bonding material can be expected to flow over any waviness. Even the protrusion of an interlayer-via can be tolerated.

Depending upon the expertise (or luck) of the manufacturing group, flatness sufficient for eutectic attach may be maintained on the top surface of the multilayer build-up if all layers below the chip mounting pad are continuous planes or if conductor tracks below are separated from the mounting pad by several continuous layers.

In any multilayer configuration, the manufacturing group should specify the chip mounting constraints.

Figure 7.6.1-4 shows examples of various configurations of semiconductor mounting on top of multiple layers.

7.6.1 (Cont.) Semiconductor Mounting

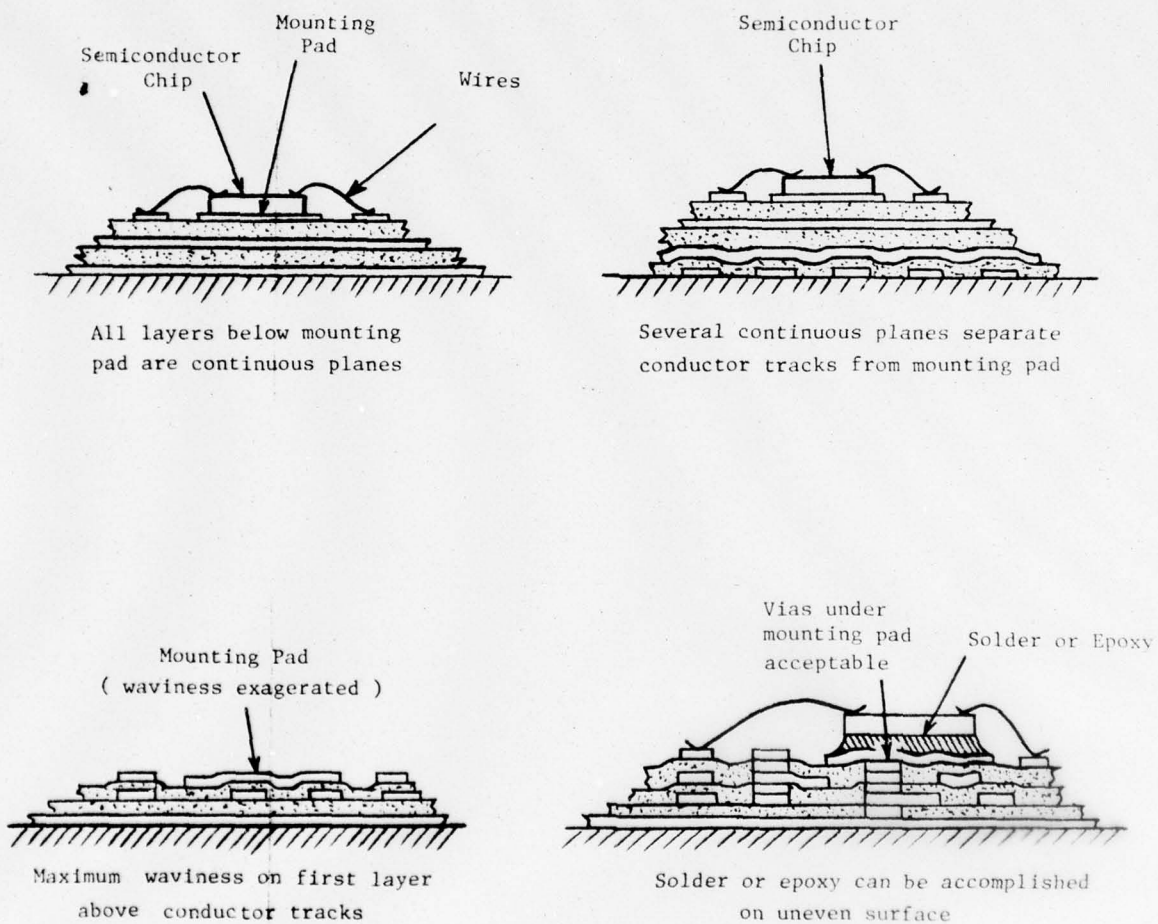
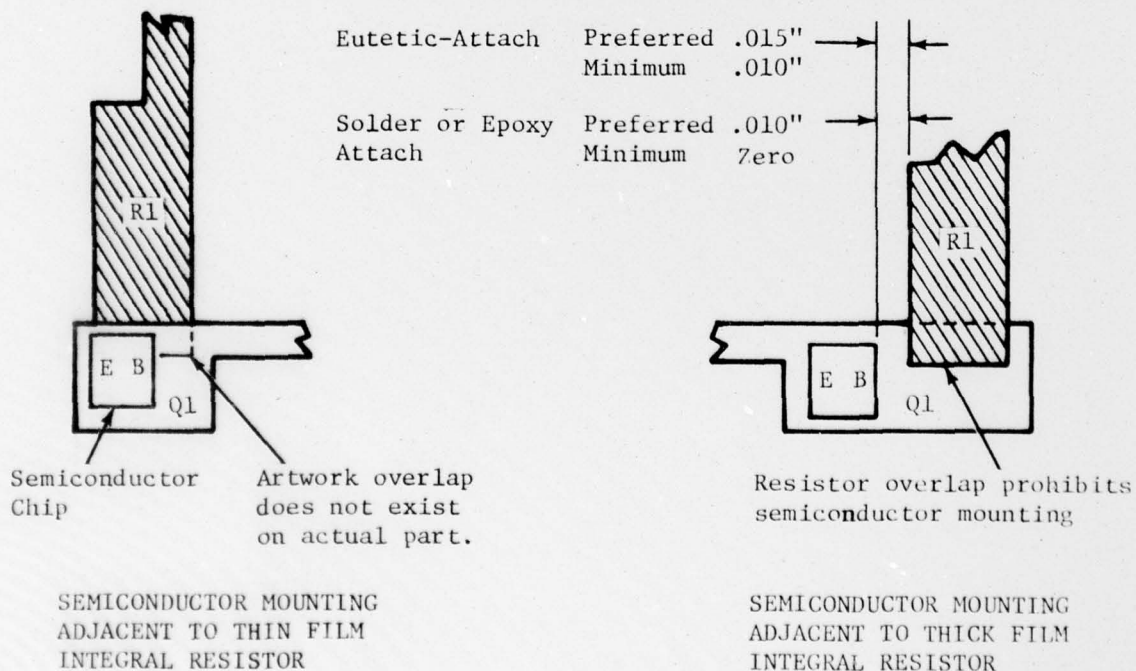


Figure 7.6.1-4 SEMICONDUCTOR MOUNTING ON TOP OF MULTIPLE LAYERS

7.6.1 (Cont.) Semiconductor Mounting

The mounting of a semiconductor chip adjacent to an integral resistor has different constraints if the substrate is thin or thick film. Thick film resistors overlap onto the top of the conductors. Thin film resistors do not. Even though in thin film pattern plating the resistor artwork overlaps the conductor, on the actual part there is no overlap. (The overlap in the artwork is to insure that the protection-from-acid extends over the edge of the conductor).

On any thin film substrate, a semiconductor may be mounted close to the edge of the resistor/conductor interface. On thick film substrates the resistor overlap prohibits this.



7.6.1 (Cont.) Semiconductor Mounting

The mounting pad for an I.C. chip should be electrically connected to the appropriate voltage. The appropriate voltage is usually the most negative voltage used for the chip function. (For many I.C. chips, GND is the most negative voltage used.)

The mounting pad for an MOS type I.C. chip may require negative or positive voltage depending on the chip specifications.

For a transistor chip the bottom surface of the chip is the collector terminal. The base and emitter terminals are in the metalization on the top surface of the chip.

For diode chips the bottom surface of the chip is the cathode terminal. The anode is in the metalization on the top surface.

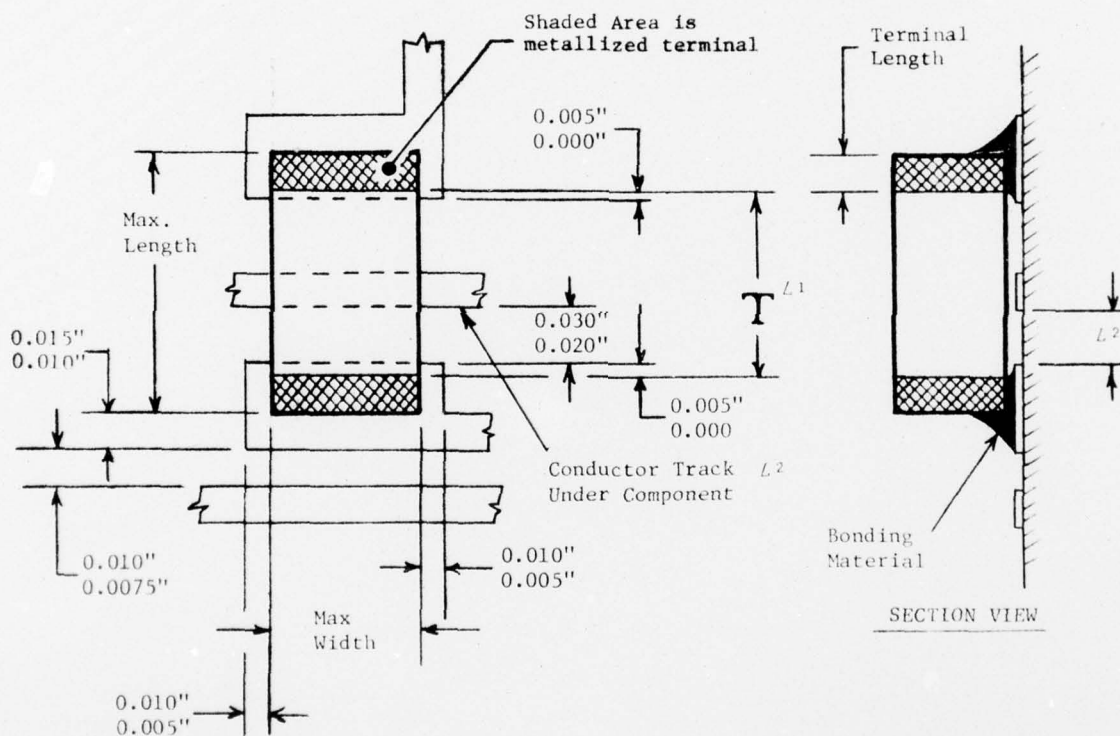
7.6.2 Ceramic Chip (Capacitor or Resistor) Mounting

The most common type of capacitor used in hybrids is the ceramic chip capacitor. It is shaped like a miniature brick, and each end is metalized to form terminals. In addition to being electrical connection points, these metalized end-terminals are used to attach the capacitor to the hybrid substrate.

The substrate conductor tracks are shaped to provide mounting pads of sufficient size to accommodate the capacitor end-terminals and the solder or conductive epoxy used for attachment. The design of the substrate mounting pads must provide for the maximum and minimum tolerances of the capacitor end-terminals.

7.6.2 (Cont.) Ceramic Chip (Capacitor or Resistor) Mounting

Resistors, in addition to being fabricated as films on the surface of the substrate, are often installed as components. One type of component resistor is a ceramic chip; shaped identical to the previously described capacitor chip. Figure 7.6.2-1 depicts a ceramic chip mounted on a hybrid substrate.



L^1 **T** is minimum distance between terminals and is equal to the minimum component length minus two times the max. terminal length.

L^2 Avoid conductor under component. If bonding material shorts across, the short cannot be seen under the component.

Note: Two numbers are shown for each dimension. The larger is preferred; the smaller is the minimum.

Figure 7.6.2-1 MOUNTING PAD DIMENSIONS FOR CERAMIC CAPACITOR OR RESISTOR

7.6.2 (ont'd.)

When a large ceramic-chip component (200 mils (5.08 mm) long or greater) is solder-attached at its terminals, the solder forms a rigid joint. The possibility exists that stress caused by the differences in expansion coefficients between the substrate and the chip may break the rigid solder joint. Figure 7.6.2-2 shows some precautions that have been used in these circumstances.

Conductive epoxy, used as the attachment at the terminals, does not form a rigid joint and can flex enough to absorb the differences in expansion.

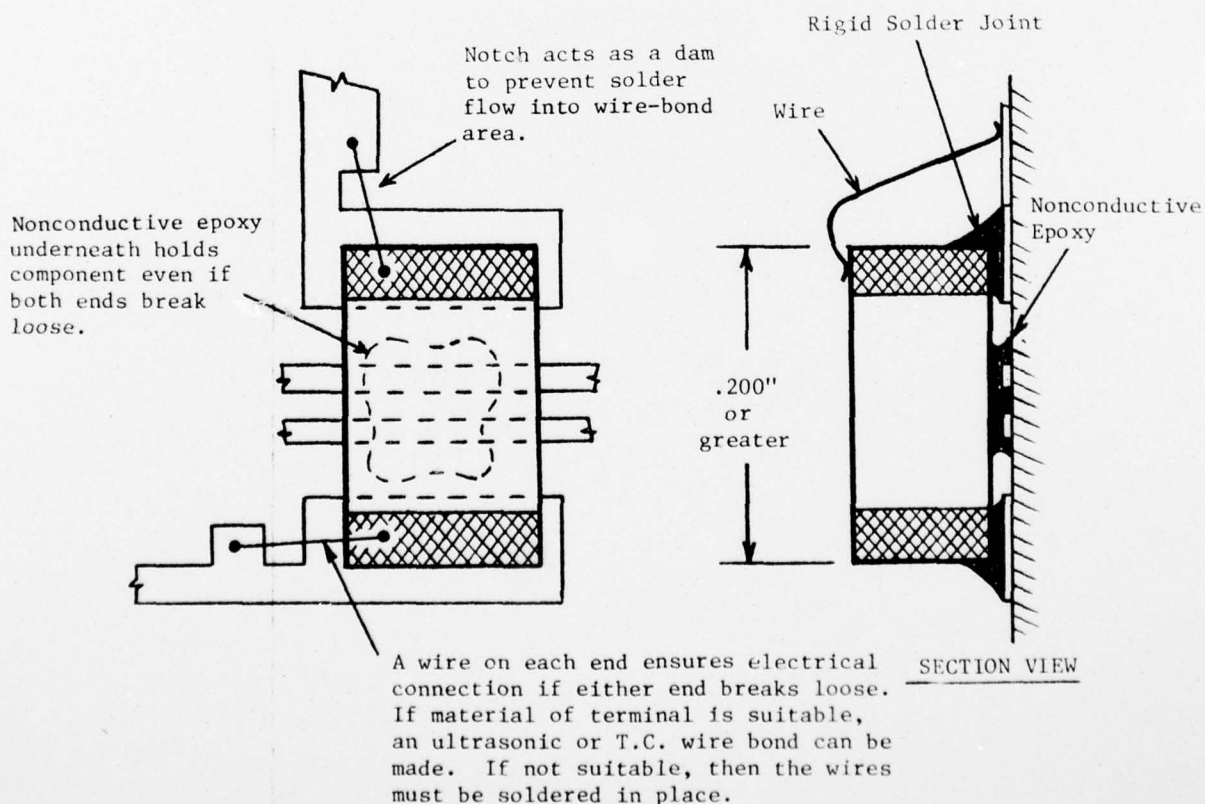


Figure 7.6.2-2 ATTACHMENT OF LARGE CERAMIC COMPONENT

7.6.3 Miscellaneous Component Mounting

Component-resistors can be purchased as thin flat chips. The chip material is typically ceramic or silicon. One or several resistors are on the top surface. The bottom surface of such a chip can be metalized to permit the chip to be solder-attached to a substrate mounting pad. When the bottom is metalized, this metal is only for mounting; it is not an electrical terminal. The substrate mounting-pad dimensions are the same as those described for semiconductor mounting-pads.

Almost any component can be mounted on a substrate. The component size and weight are the primary limiting factors.

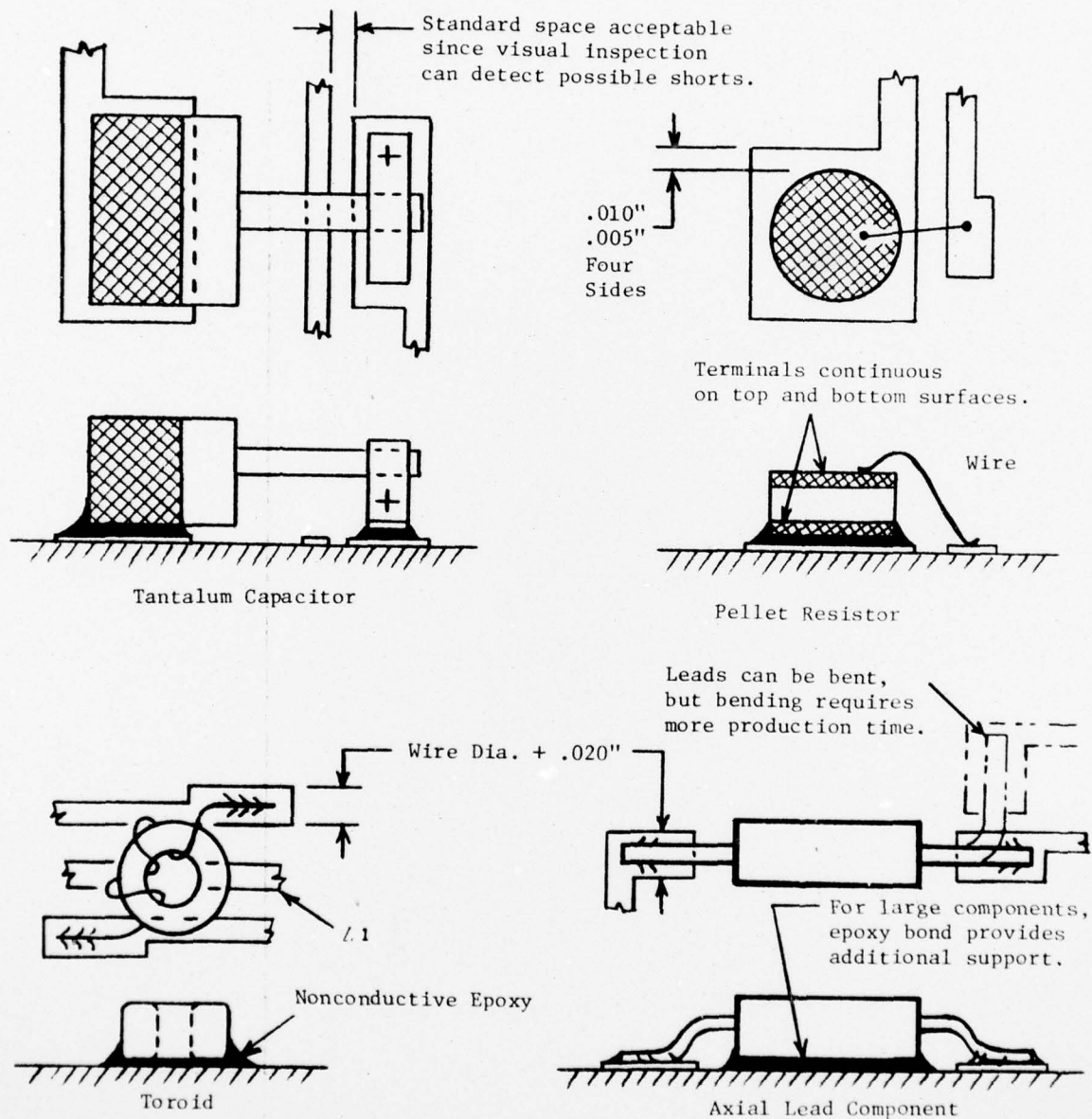
The space between components should accommodate location tolerances and the flow of the component bonding material. 15 mils (0.281 mm) is usually sufficient.

Small substrate assemblies are often mounted on larger ones. Epoxy or solder is usually the method of attachment. The smaller assemblies are typically pretested prior to being installed.

Reminder: The maximum height of any component or subassembly must remain below the cover of the package.

Several miscellaneous component configurations are noteworthy. Figures 7.6.3-1 and -2 illustrate plan and elevation views of the most common.

7.6.3 (Cont.) Miscellaneous Component Mounting



L1 The area under a toroid may be signal tracks, a mounting pad connected to gnd, an unconnected mounting pad, or no metallization of any kind. The electrical circuit dictates the constraints.

Figure 7.6.3-1 MISCELLANEOUS COMPONENT MOUNTING

7.6.5 (Cont.) Miscellaneous Component Mounting

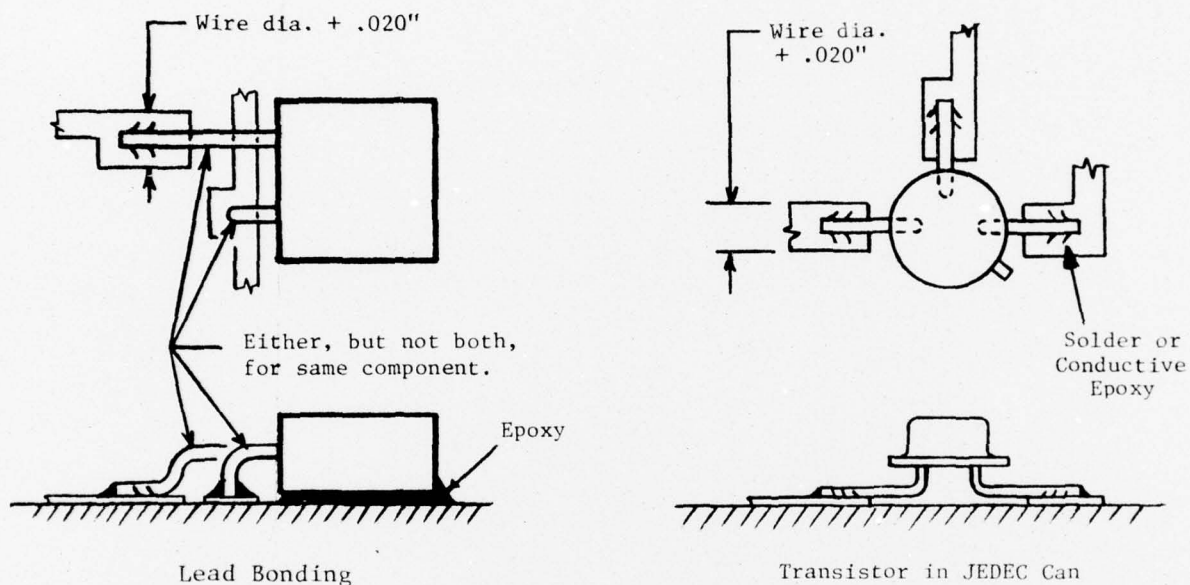


Figure 7.6.3-2 ADDITIONAL MISCELLANEOUS COMPONENT MOUNTING

7.6.4 Beam Leaded Component Mounting

Beam leaded semiconductor chips are intended to be mounted face down and the leads TC bonded to the substrate mounting pads. The beams are typically gold, 3 mils (0.0762 mm) to 5 mils (0.127 mm) wide and 0.5 mils (0.0127 mm) thick. Power devices sometimes have wider beams. The pattern of mounting pads are designed to match the location of the beams.

Figure 7.6.4-1 shows typical configurations of diode and transistor chips viewed from the back side (i.e., looking perpendicular to the substrate surface).

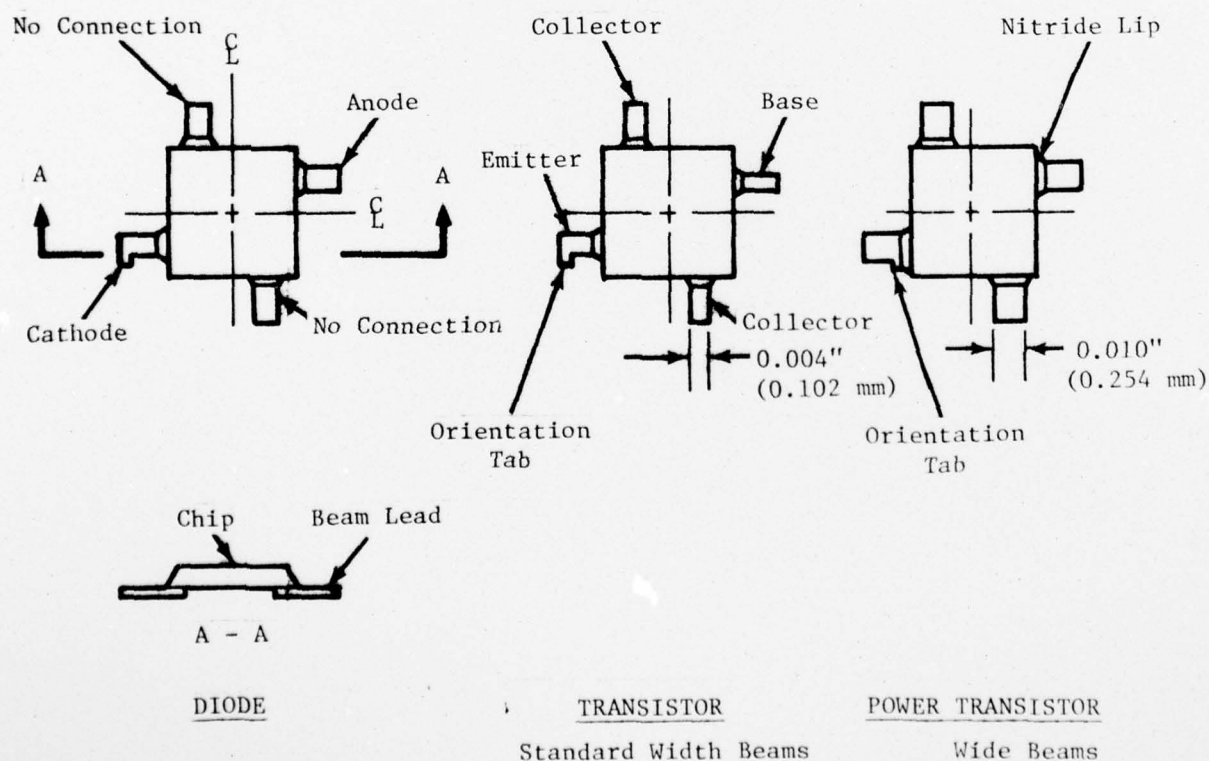


Figure 7.6.4-1 BEAM-LEADED DIODE AND TRANSISTOR CHIPS

7.6.4 (Cont.) Beam Leaded Component Mounting

Note that the beams are not located on the chip center lines. The off-center rotation can be counter clockwise (as shown) or clockwise. The beam lead identification as shown is not necessarily a universal standard; other arrangements may be used. It is necessary to check the individual chip manufacturer's specification to determine chip layout and beam identifications.

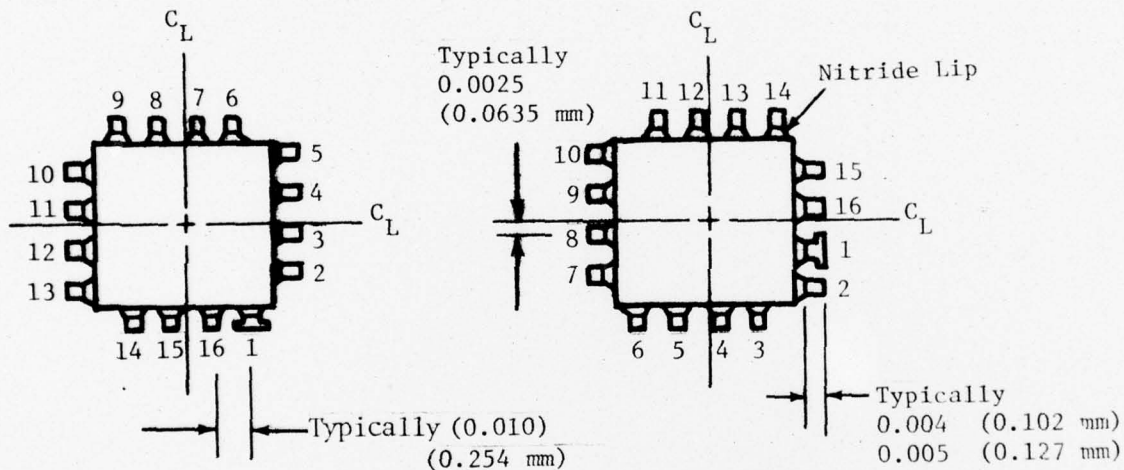


Figure 7.6.4-2 TYPICAL BEAM-LEADED INTEGRATED CIRCUITS

Note that also in integrated circuits the beams are not located on the chip center lines. Both clockwise and counterclock beam rotation and numbering are shown.

The substrate mounting pads should have the same center to center spacing as the beams but not necessarily the exact width. Mounting pads 5 mils (0.127 mm) wide on 10 mil (0.254 mm) centers will suffice for most chips. However, some power transistors have beams as wide as 20 mils (0.508 mm) with lengths of 9 mils (0.229 mm).

7.6.4 (Cont.) Beam-Leaded Component Mounting

5 mil pads on 10 mil centers is standard fabrication criteria for thin film substrates but these dimensions are difficult with thick film. For thick film, this narrow width should be maintained for only short distances; the conductor lines should be widened as close to the mounting pads as possible. This enlargement can be accomplished using a sunburst pattern.

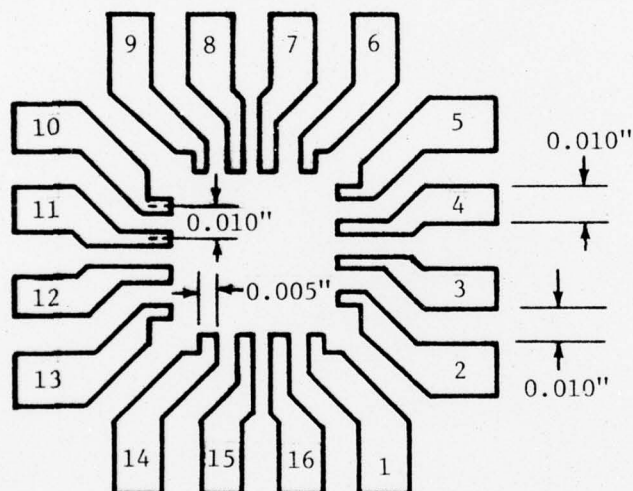


Figure 7.6.4-3 TYPICAL BEAM LEAD MOUNTING PADS ON THICK FILM SUBSTRATE

Due to the thick film paste spreading when it is squeezed through the screen, the actual width of a thick film line is usually slightly wider than the line in the screen image. The artwork is sometimes compensated to take this spreading into account. The manufacturing group should be consulted to determine the exact dimensions for the artwork.

7.6.4 (Cont.) Beam Leaded component Mounting

The section view shown in Figure 7.6.4-4 shows the typical configuration of a beam leaded chip after bonding; and depicts the relationship of mounting pads to chip size.

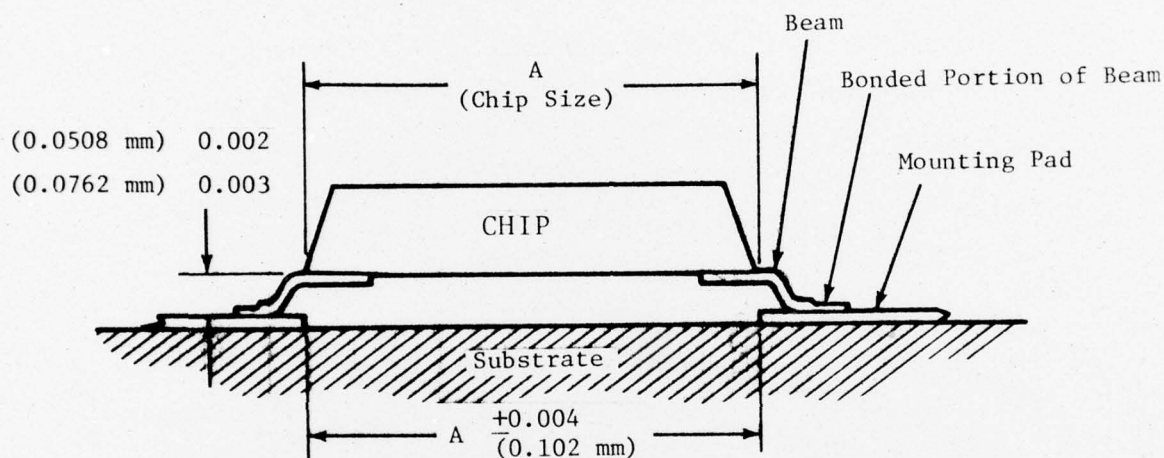


Figure 7.6.4-4 SECTION VIEW OF BEAM-LEADED CHIP AFTER BONDING

After bonding, the body of the chip is typically raised off of the substrate surface as shown. (This raising of the chip is often referred to as "bugging.")

It is recommended that the area under the body of the chip be free of conductor tracks, but because of the bugging, this is not a rigid rule. Care should be exercised if a track is to be routed in this area. Referring to Figure 7.6.4-3, if pad number 1 were to be connected to some pad (other than 2 or 16) by a conductor track across the open area in the center of the pattern, then the clearance between that interconnecting track and pads 16 and 2 must be maintained. The same caution applies to any of the corner pads.

7.6.4 (Cont.) Beam Leaded Component Mounting

One mounting pattern concept is noteworthy. A sunburst pattern can sometimes be designed to accommodate more than one chip, each having a different number of beams. Figure 7.6.4-5 depicts a pattern used for both a 42 and a 50 beam chip.

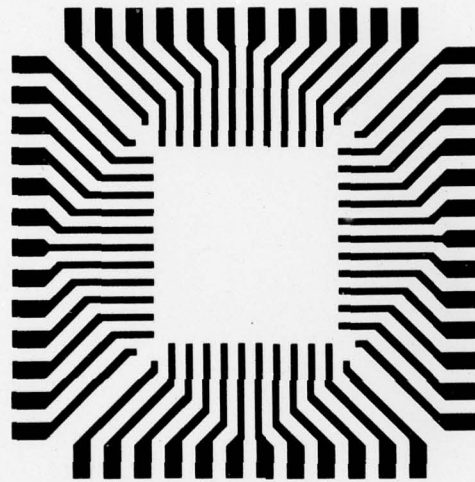


Figure 7.6.4-5 ONE MOUNTING PATTERN FOR BOTH 42 AND 50 BEAM CHIPS

In Figure 7.6.4-5 the 50 beams are bonded to the ends of the corner pads. The row of bonds on the other pads are in line with the bonds on the corner pads. The 42 beams are bonded on the inner ends of the 42 mounting pads. This concept can be extended to accommodate 34 beams, 26 beams, and 18 beams.

Since the diode and transistor chips have only one beam on each side none of the beams are adjacent; making it possible to widen each mounting pad. However, widening of the thick film mounting pads might be restricted by bond testing procedures.

7.6.4 (Cont.) Beam Leaded Component Mounting

After the beams are bonded, the strength of the bond can be tested by one of two methods. One test method places no restrictions on the mounting pad sizes, but the other method restricts the size of thick film mounting pads.

The most commonly used bond strength test is a sampling destructive test. The test consists of adhesive-attaching a wire or hook to the back side of the installed chip; then pulling the chip away from the substrate until all the beams break. The criterion for acceptance is that a certain minimum force be required to break the beams. This testing method places no restrictions on the mounting pad sizes.

Another test might be used that does put restrictions on the size of thick film mounting pads. That method tests the bond strength by individually pushing the bonded portion of each beam using a sharp wedge. This test requires that the wedge push against either the side or the end of the bond.

On thin film pads, the sides of the bonded portion are typically raised above the surface of the mounting pad making the sides accessible for the push test. On thick film substrates, because the pad material is thick, the bonded portion of the beam will become completely imbedded into the pad if the pad is significantly wider than the beam. Imbedded beams cannot be push tested.

To avoid imbedding the beams, thick film mounting pads should not be more than 2 mils (0.0508 mm) wider than the beam. The size and shape of the push tool might also influence the mounting pad configuration so the manufacturing group should be consulted.

7.6.4 (Cont.) Beam Leaded Component Mounting

Because beam leads are all TC bonded to the substrate, the bonds are more reliable on thin film than on thick film. The thin film conductor material is compact, pure gold; whereas thick film conductors are porous gold mixed with glass frit. If the surface of the thick film mounting pad has too much glass, no TC bond can be made. (Ultrasonic bonding can break through the glass.)

Excessive glass on the mounting pads is more prevalent for multilayer than single layer substrates. There are two reasons for this prevalence. If the mounting pads are on the top layer, the glass in the lower dielectric layer tends to combine with the glass in the conductor paste creating an excessive amount of glass in the conductor. If the mounting pads are in an area devoid of multiple layers, but multiple layers are present in other areas of the substrate, then the additional firing cycles required for the multiple layers tend to bring the glass to the surface of the mounting pad.

Excess glass can be removed by gentle abrasion, but this introduces another manufacturing process step. The manufacturing group should be consulted to establish the constraints for beam lead bonding on multilayer thick film substrates.

7.7 WIRE-BONDING GUIDELINES

Two methods are commonly used to install interconnecting wires within hybrid microcircuits. These two methods are thermo-compression bonding (often referred to as "TC" bonding) and ultrasonic bonding (often called "stitch-bonding").

TC bonding installs each end of an uninsulated gold wire in the designated place by applying heat and vertical pressure. The designated place on a substrate conductor track is called a bonding pad. Ultrasonic bonding installs either an aluminum or gold wire by scrubbing the ends into place at an ultrasonic frequency. (Ultrasonic attachment of a gold wire requires some application of heat as well, but not as much as TC bonding requires.)

The selection of either method involves tradeoffs concerning wire cost, material compatibility, electrical conductivity, wire strength, and availability of installation equipment. (Section 6.3 briefly describes wire-bonding processes and equipment.)

The most commonly used wire diameter is 1 mil (0.0254 mm). Larger diameters can be used as required. Production efficiency is enhanced when all bonded wires within any one hybrid are the same material and size. But where electrical or other requirements dictate varying sizes, they can be used. It is not uncommon that aluminum bonds are used at all points internal to the substrate, and the connections from the substrate to the package leads are made with gold TC bonds. The rationale for this combination is that aluminum wires are best on the aluminum terminal pads of the semiconductors, while the higher conductivity of the gold wires improves the connections

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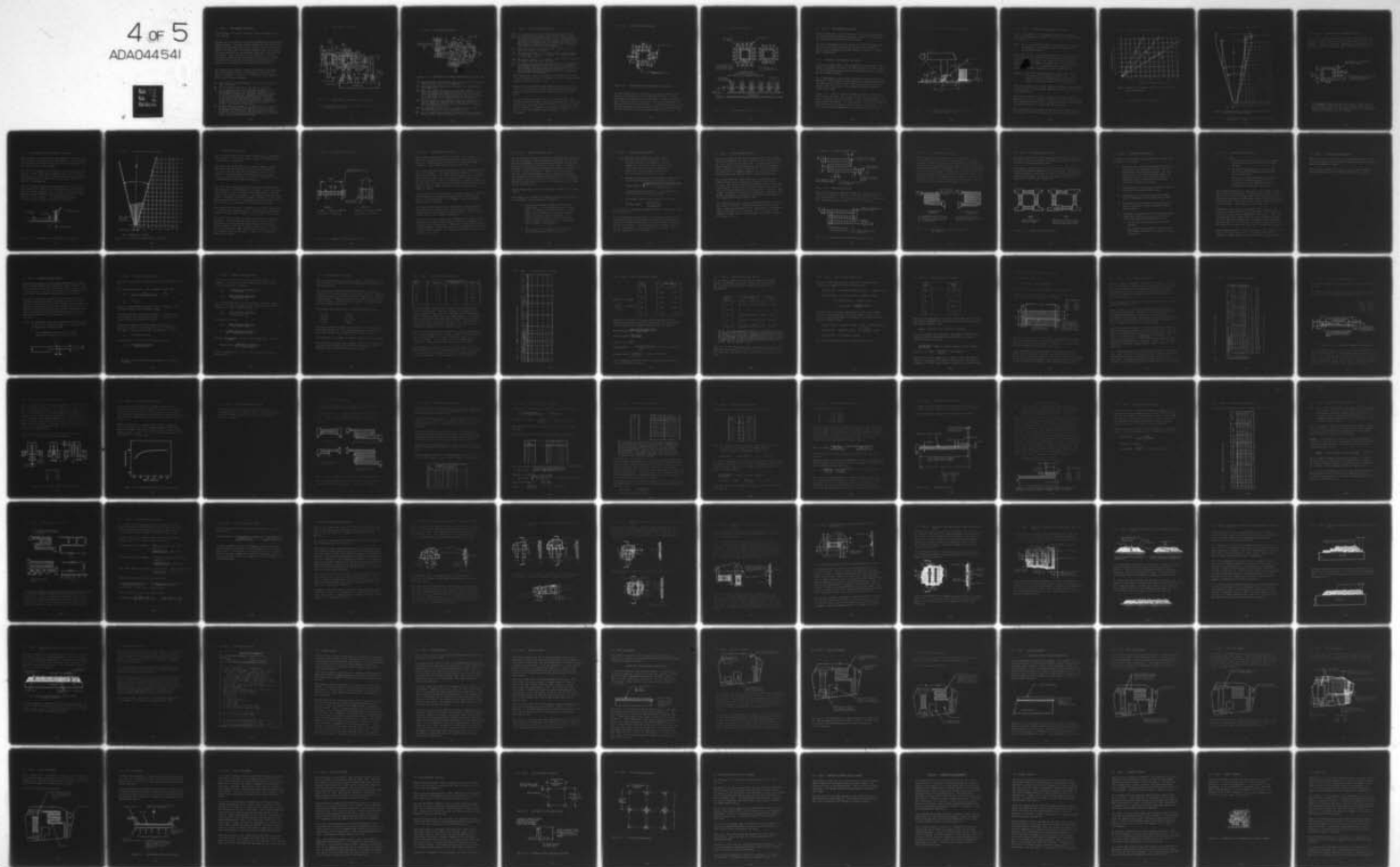
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7.7 (Cont.) WIRE-BONDING GUIDELINES

to the package. Of course, the lower cost of aluminum is not to be ignored.

Problems have occasionally arisen when aluminum and gold have been bonded together. (The name "purple plague" has been given to one deleterious substance that has been seen to form in the joint.) Studies have shown that the various problems occur where certain excessive temperatures, environmental conditions, and impurities are present. These conditions are not difficult to avoid in manufacturing and testing, but before any design specifies the two metals in conjunction it should be ascertained that the processes to be used do not contribute to such problems.

The following text explains various wire-bonding constraints. The circled numbers refer to configurations of bonded wires shown in Figures 7.7-1 and 7.7-2. These constraints apply to both TC and ultrasonic bonding.

- ① Since the wires are uninsulated, no two wires should ever cross each other.
- ② No wire should extend across the body of the chip.
- ③ A wire should not be installed from a terminal on one semiconductor directly to a terminal on another. An intermediate pad on the substrate should be provided. Because the semiconductor terminals are usually small, it is very difficult (and often impossible) to make a second bond on one semiconductor terminal. Therefore, if one of two such chips ever needed to be replaced, the second chip would also have to be replaced because its terminal could not be bonded again.
- ④ Bonding from one terminal of a semiconductor chip directly to another terminal of that same chip is to be avoided. An intermediate bonding pad should be provided on the substrate. This is to avoid the possibility of the center portion of the wire sagging down and shorting to metallization on the top surface of the chip.

7.7 (Cont.) WIRE-BONDING GUIDELINES

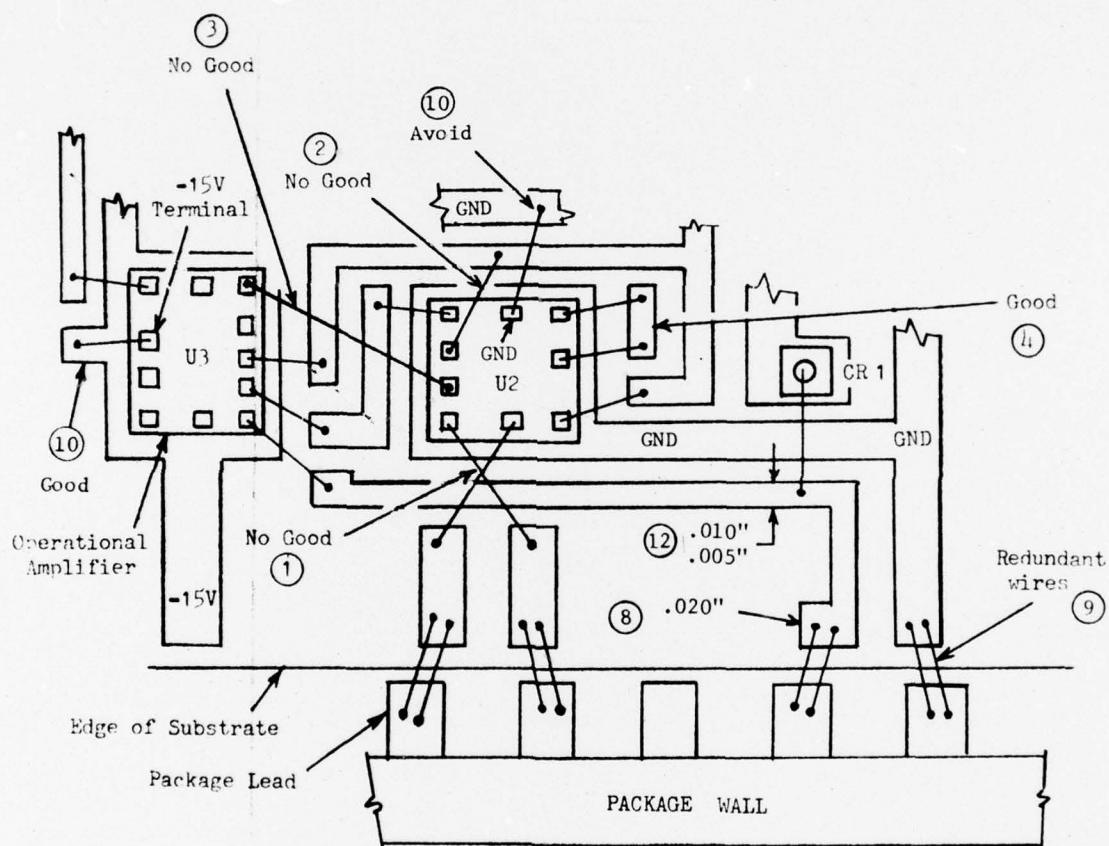


Figure 7.7-1 WIRE-BONDING CONSTRAINTS FOR 1 MIL WIRE ^{L1}

^{L1} The requirements for larger wires should be specified by the manufacturing group.

7.7 (Cont.) WIRE-BONDING GUIDELINES

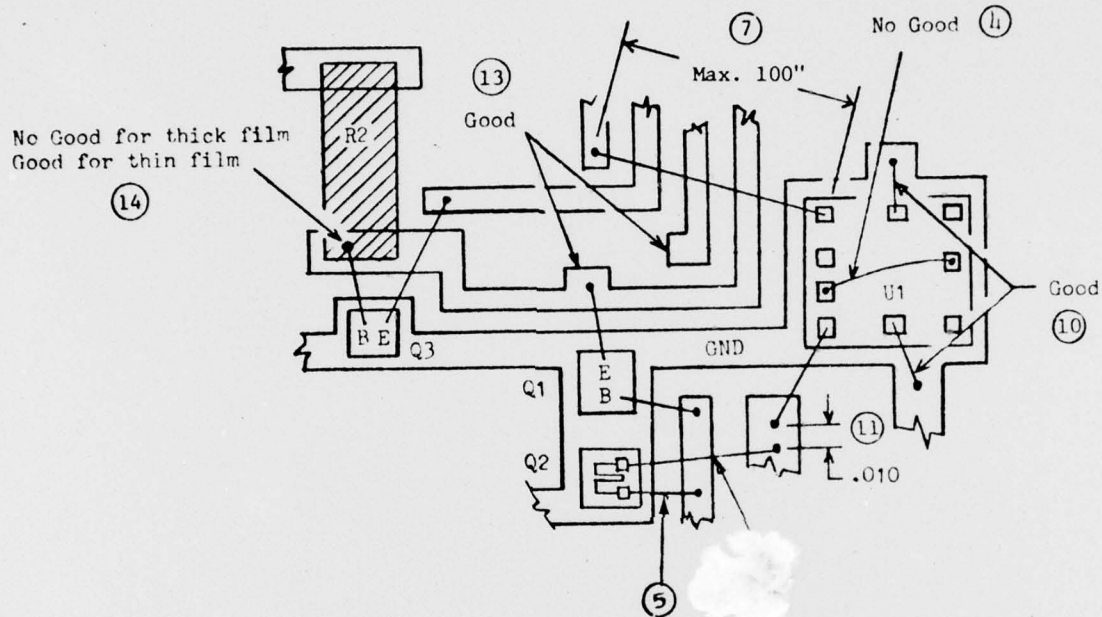


Figure 7.7-2 ADDITIONAL WIRE-BONDING CONSTRAINTS FOR 1 MIL WIRE

- ⑤ Where possible, bonding pads should be close to the component from which the wire is to be connected.
- ⑥ Avoid any other conductor track between the component and the bonding pad.
- ⑦ When ⑤ cannot be achieved, the maximum length of a 1 mil gold or aluminum wire should be 100 mils (2.54 mm). This criterion ignores the length due to the loop of the wire. It is the dimension seen when viewing the substrate in the usual plan view, (i.e., perpendicular to its surface).
- ⑧ Wherever possible, the conductor track, from which a wire will be bonded to a package lead, should be enlarged to form a bonding pad 20 mils x 20 mils (0.508 mm). Such pads are often called "exit pads."
- ⑨ For improved reliability, two redundant wires are often installed between exit pads and package leads.
- ⑩ An I.C. mounting pad should be connected to the appropriate voltage track. The corresponding voltage-terminal on top of

7.7 (Cont.) WIRE-BONDING GUIDELINES

- (10) the chip must also be wire bonded to the voltage track.
(Cont.) This bond on the voltage track should be made as close as possible to the mounting pad. A tab is often extended from the mounting pad to provide such a close bonding pad. The reason for bonding close to the mounting pad is that a difference in voltage might exist between two widely separated points along the voltage track. Such a difference might adversely effect the chip function.
- (11) The space between two adjacent bonds, on the substrate, should be 10 mils (0.254 mm).
- (12) The preferred width of a conductor track on which a bond is to be made is 10 mils (0.254 mm). The minimum width is 5 mils (0.127 mm).
- (13) Where space permits, the conductor track should be enlarged (>0.010) to provide easier bonding.
- (14) On a thick film substrate, the overlap area of an integral-resistor and conductor cannot be used for wire bonding. On any thin film substrate a bond can be made in this area. (In thin film pattern plating, the artwork-overlap exists only to insure protection from etching acid. No overlap exists on the finished part).

Wire bonding on a thick film multilayer substrate has an additional consideration, that is, whether or not a wire bond should be made directly on top of a via.

Whenever the overflow-via contact method is used (See Section 7.9.2), it is to be expected that there should be no wire bond directly on top of a via, since a depression exists at that point.

In some design groups where there is a suspicion that some filled-vias may be slightly recessed, there might be a constraint prohibiting a wire bond directly on top of a filled-via. When such a constraint is imposed, an adjacent bonding pad (10 mil x 10 mil {0.254 mm} minimum) must be provided. Figure 7.7-3 is an example.

7.7 (Cont.) WIRE-BONDING GUIDELINES

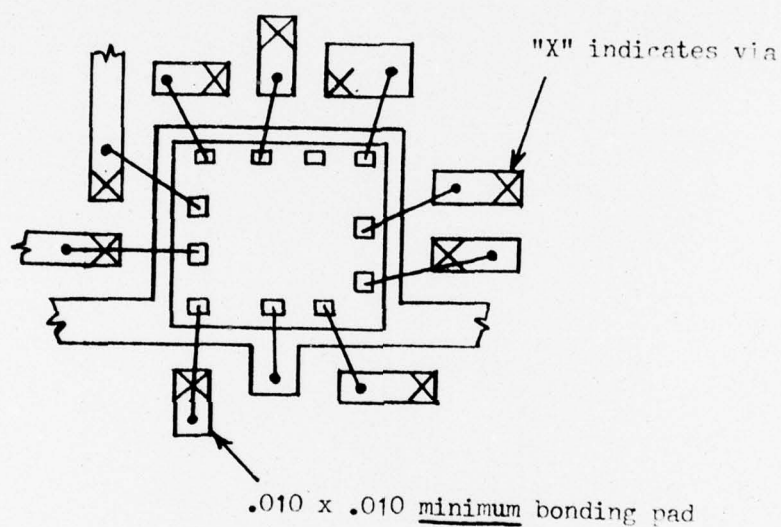


Figure 7.7-3 WIRE-BONDING PADS ADJACENT TO FILLED-VIAS

In other design groups, where there is a high confidence in the flatness of filled-vias, no such prohibition exists. In fact, one substrate configuration is noteworthy in which all bonds are made directly on top of filled-vias. In this configuration, the top surface of the multiple layers is a continuous dielectric layer. The only conductors on the top surface are the chip mounting pads and the filled-vias, which protrude through the dielectric. Each

7.7 (Cont.) WIRE-BONDING GUIDELINES

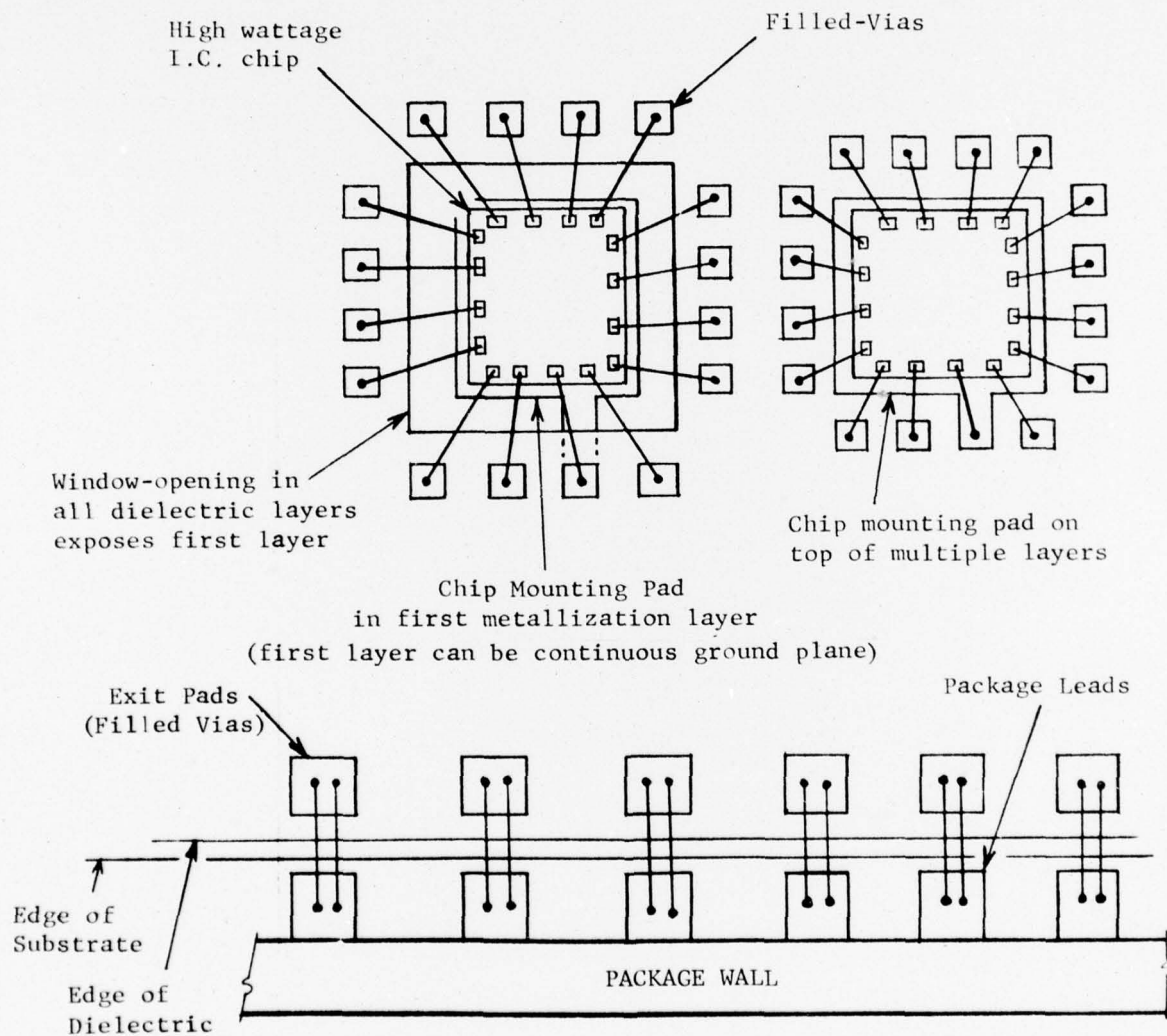


Figure 7.7-4 WIRE-BONDS DIRECTLY ON TOP OF FILLED-VIAS

7.7 (Cont.) WIRE-BONDING GUIDELINES

of the filled-vias is a wire bond pad. All of these bonding pads are located either around the perimeter of the I.C. chips or at the edge of the substrate forming exit pads.

In such a configuration, after die attach, the wire bonding pads are the only visible metallization on the entire substrate. Errors in wire bonding are greatly reduced. Figure 7.7-4 shows this configuration.

7.7.1 Ultrasonic Wire-Bonding Constraints

Ultrasonic bonding imposes some unique design requirements. The unique requirements are due to the shape of the tool, the direction of tool movement, and the direction from which the tool is viewed by the assembly operator.

It is advantageous to the assembly operator to have the option of bonding in either sequence (chip bond first, substrate bond second; or substrate first, chip second). Wherever possible, the design should permit this option. The necessary clearances should be taken into account.

Figure 7.7.1-1 depicts a typical bonding situation. It shows the first bond on the chip, the second on a substrate bonding pad. It can be seen that since the operator's line-of-sight cannot be at an angle greater than $\approx 60^\circ$, it is unacceptable to have any obstruction that would require a greater angle in order to be seen over. If the chip were a high component, the second bond could not be so

7.7.1 (Cont.) Ultrasonic Wire-Bonding Constraints

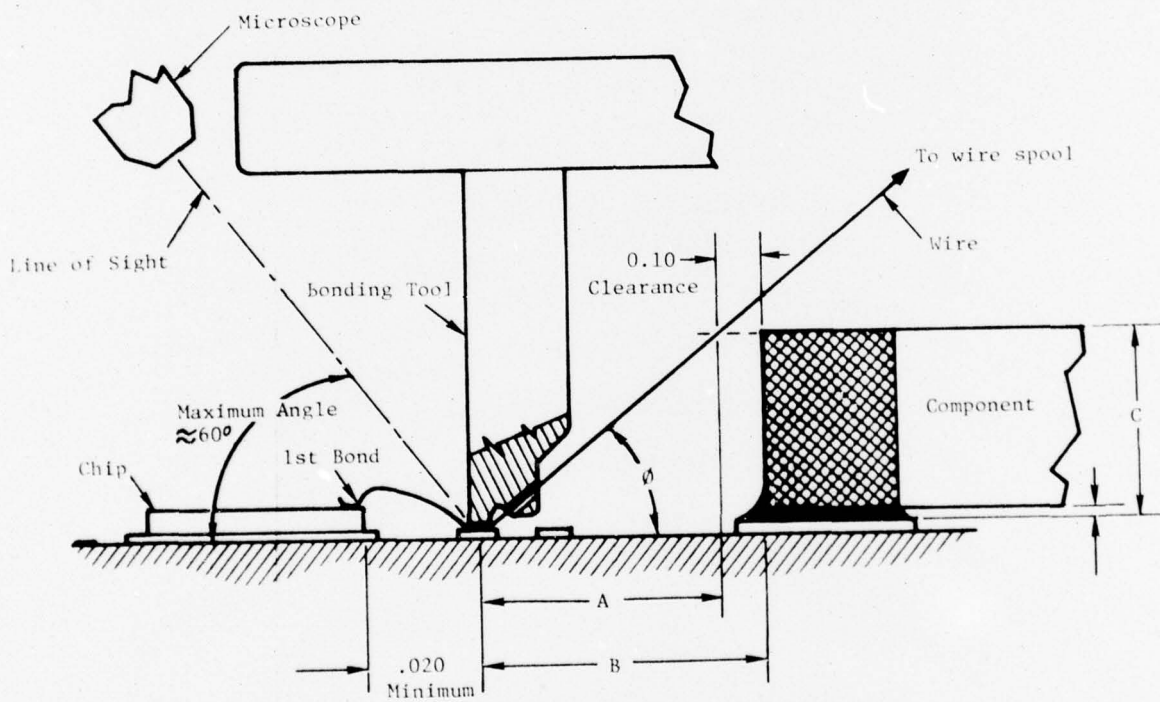


Figure 7.7.1-1 CLEARANCES REQUIRED IN FRONT AND BACK OF ULTRASONIC BONDING TOOL

7.7.1 (Cont.) Ultrasonic Wire-Bonding Constraints

close. For example, if the component shown, having height C, were interchanged with the chip, it would be such an unacceptable obstruction.

Note: 60° is a conservative angle. Larger angles can usually be accommodated. The manufacturing group should specify the maximum allowable.

On the back side of the bonding tool, there can be no obstruction that would interfere with the wire coming from the wire spool on the border. The angle of the wire varies for different bonding tools. The common wire angles are: 30° , 45° , and 60° . The graph in Figure 7.7.1-2 provides handy reference for determining the necessary clearances for these common angles.

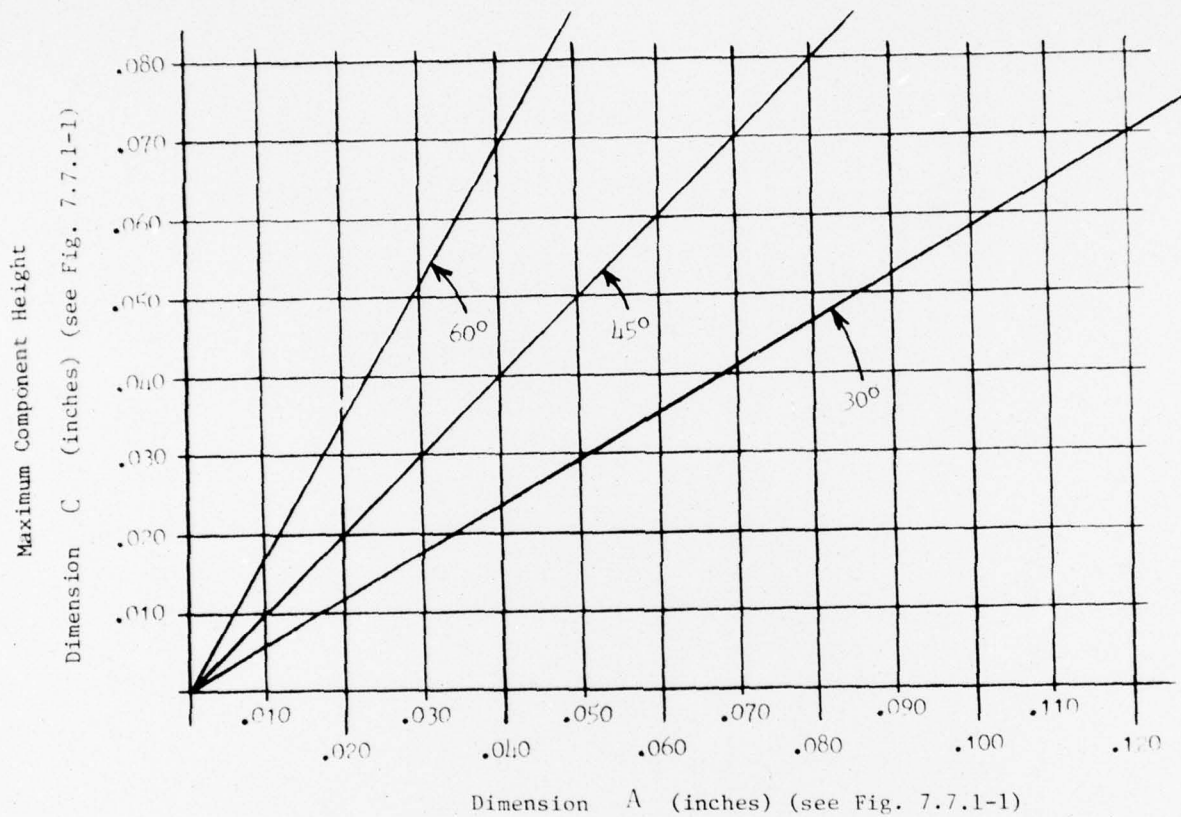
Reminder: The first bond must always be made closest to the microscope, the second bond farthest away. The optional sequence mentioned above requires the substrate to be rotated relative to the microscope.

Since the package wall is higher than any component, consideration of these angles is particularly important for wire bonds close to the package wall.

The size and shape of the tool, as viewed from the operator's direction, is also a variable. Figure 7.7.1-3 shows some typical tool dimensions and can serve as a handy reference for determining clearances required, as viewed from the microscope.

When performing wire bonding, the operator must always allow for the parallax involved in judging the surface bond point while the

7.7.1 (Cont.) Ultrasonic Wire Bonding Constraints



REMINDER: Dimension B (actual component location, see Fig. 7.7.1-1) is .010 greater than dimension A

Figure 7.7.1-2 GRAPH OF 30°, 45°, 60° ANGLES

7.7.1 (Cont.) Ultrasonic Wire Bonding Constraints

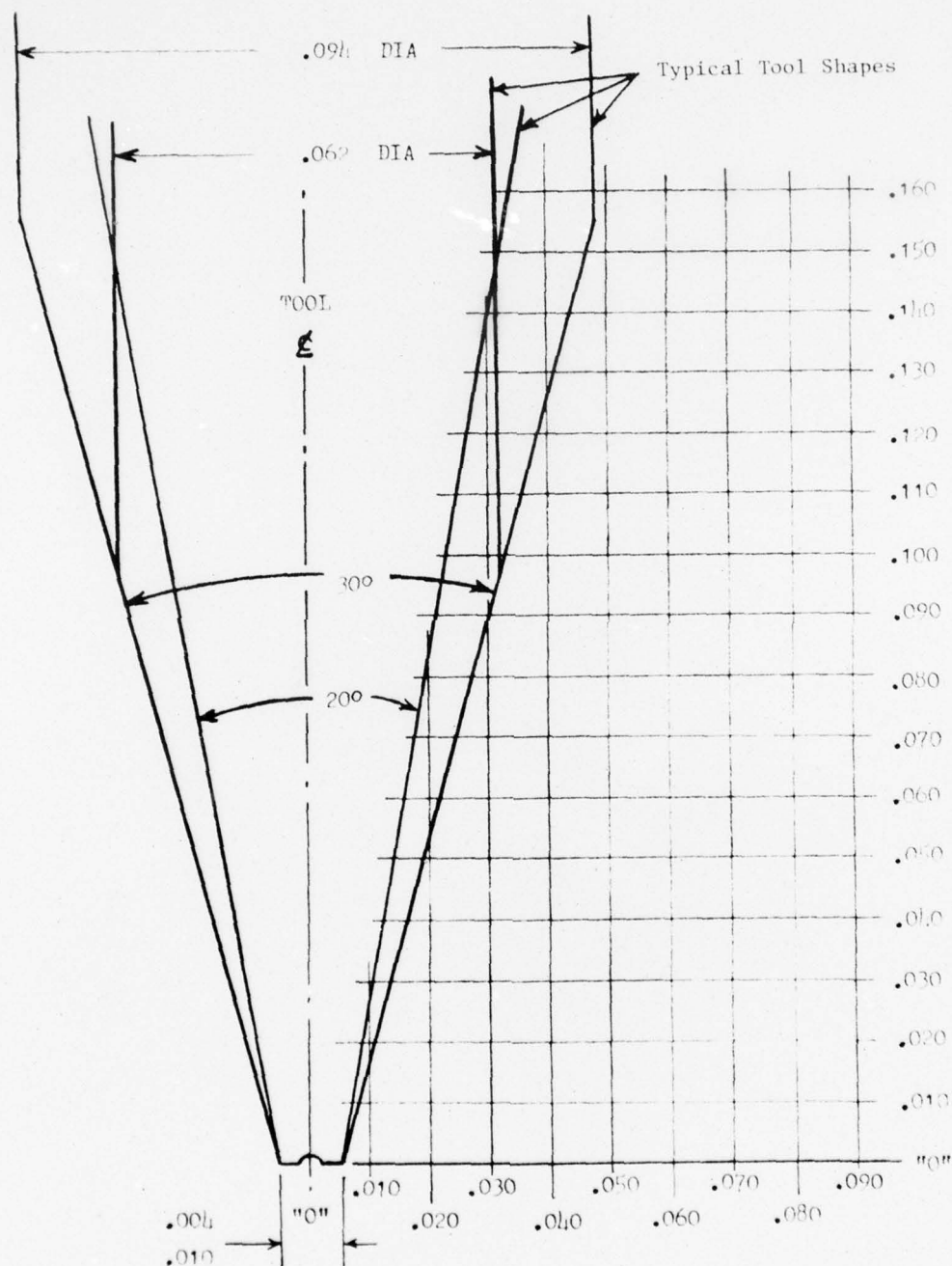
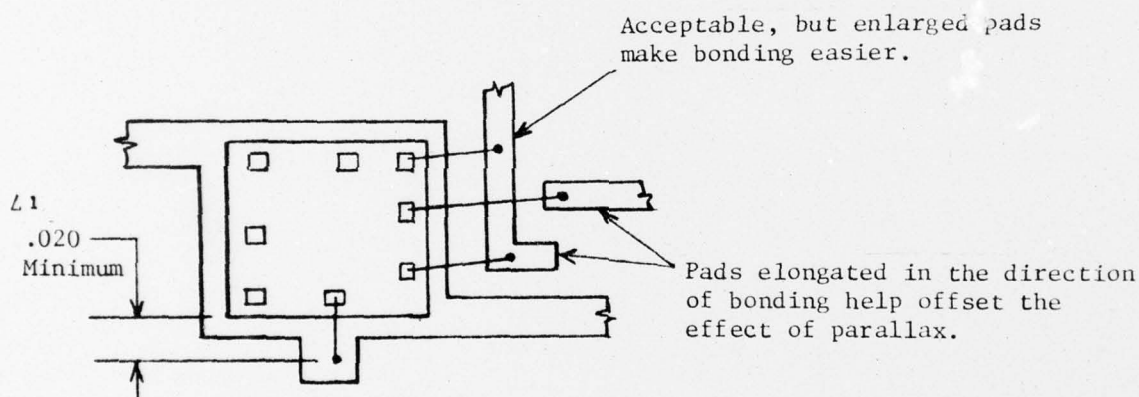


Figure 7.7.1-3 FRONT VIEW OF TYPICAL ULTRASONIC BONDING TOOLS (DIMENSIONS IN INCHES)

7.7.1 (Cont.) Ultrasonic Wire Bonding Constraints

tool is in a raised (search level) position. When bonding, the operator's view is always in line with the direction of the tool movement. Therefore, providing a bonding pad, elongated in the direction of the tool movement, makes the operator's task easier.



- ^{L1} The minimum distance from the edge of a chip to the bond on the substrate should be 20 mils (0.508 mm). When the first bond is made on the chip, this space allows for the wire loop. When the first bond is on the substrate, this space allows for clearance of the back side of the tool.

7.7.2 Thermocompression Wire-Bonding Constraints

The differences in layout design requirements between ultrasonic and TC bonding are determined by three factors: the tool shape, the direction from which the wire is fed to the tip of the tool, and the direction of tool movement.

The typical TC bonding tool is shaped in a 30° cone, with a flat bottom 7 mils (0.190 mm) in diameter. The 1 mil (0.0254 mm) diameter wire is fed to the flat bottom tip through a vertical hole directly down the center line of the cone. The tool is movable in any direction.

The only clearance required when making the first bond is that sufficient for the 30° cone. If the second bond is close to the edge of the same component, then 12.5 mils (0.317 mm) minimum allowance should be made for the curvature of the wire. (See Figure 7.7.2-1.) Figure 7.7.2-2 can be used as a handy reference for the clearance required for the 30° cone.

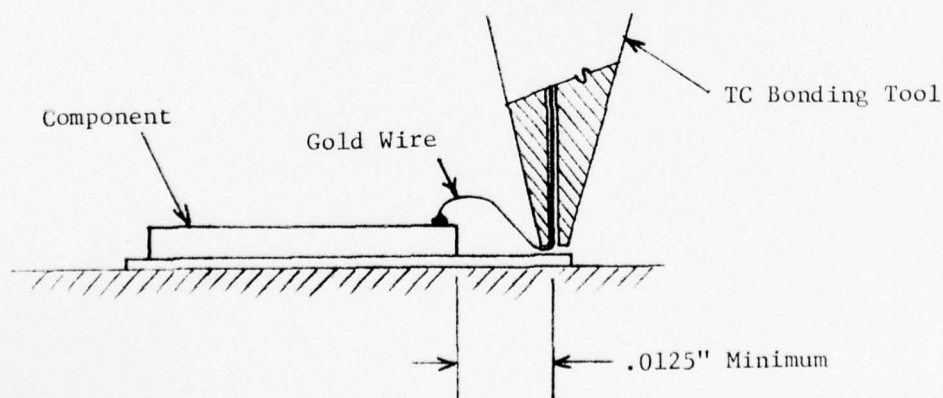
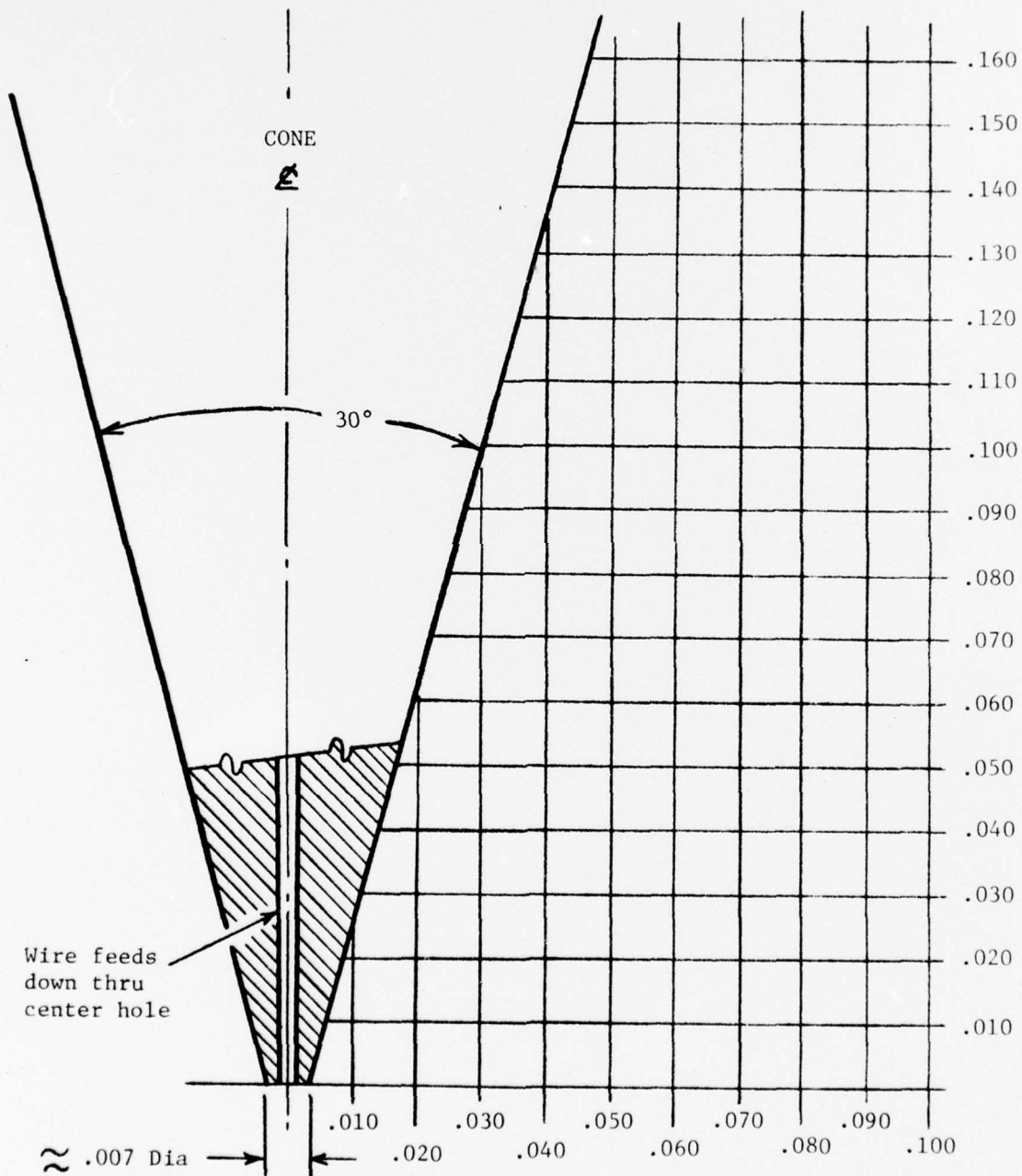


Figure 7.7.2-1 CLEARANCE FOR TC BOND CLOSE TO COMPONENT

7.7.2 (Cont.) Thermocompression Wire Bonding



Note: Dimensions are in inches.

Figure 7.7.2-2 TYPICAL TC BONDING TOOL (30° CONE)

7.8 INTEGRAL RESISTOR DESIGN

The resistance value of an integral film resistor is dependent on three factors: the resistor cross-section, its length, and the resistivity of its material.

The resistivity of the material is rated in ohms-per-square. This means that the resistance of every square-shaped area of the material will have the rated value. The size of the square is of no consequence in determining the resistance. (10 mils x 10 mils (0.254 mm) or 50 mils by 50 mils (1.27 mm) configurations will have equal resistance.)

The total cross-section (width and thickness) actually affects the resistance; but the thickness is assumed to always be constant and therefore is not considered in the calculations. Only the width is used in the calculations. The variations due to fluctuations in thickness are lumped together with other variables into the resistivity tolerance. The manufacturing group should specify this tolerance as a percentage of the resistivity rating.

The length of the resistor is defined as the distance between its two end terminals (conductor pads). Later text will explain the allowances to be made for bends or curves in the resistor shape.

The total resistor can be conceived as many squares accumulated in series. The width and the length of the resistor must be determined such that the length will add up to the number of squares needed to give the desired resistance value. The length will be less than one square long whenever the desired value is less than the value of one square. Figure 7.8-1 graphically depicts this concept.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

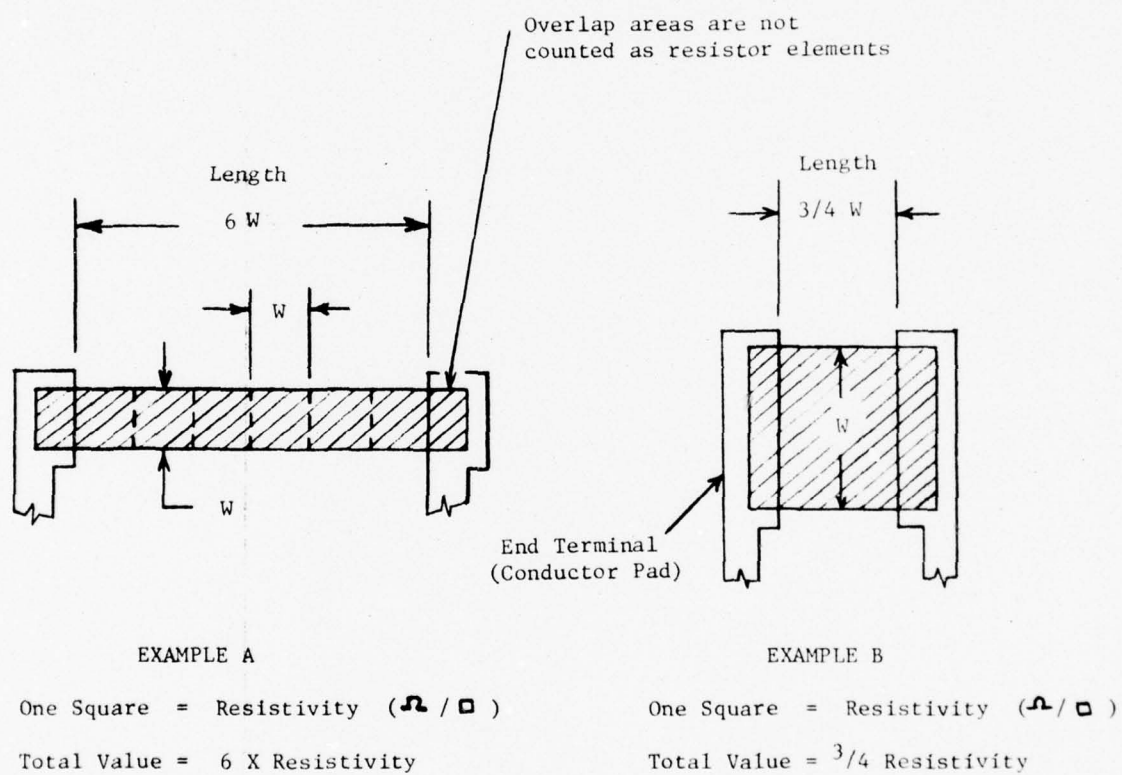


Figure 7.8-1 EXAMPLES OF RESISTOR DESIGN CONCEPT

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Due to manufacturing and material variables, it is almost impossible to consistently achieve the exact value of resistivity. Therefore, compensation must be made for all the predictable tolerances. This compensation is made in two parts.

The resistor is intentionally designed to a lower value than called for on the schematic. The length and width dimensions are calculated to ensure that even if the maximum increase due to tolerance does occur, the value will still be less than or equal to the desired final value. After the substrate is completely fabricated, the resistance is raised to the final value by cutting the resistor width to a lesser dimension which, in effect, increases the number of squares.

This cutting of the resistor width is called "trimming." The value of the resistor is continuously monitored while the trimming process is being performed. The trimming is shut off when the desired value is reached.

The processing tolerances may be either plus or minus; therefore, the design of the resistor must also provide the capability of compensating for the maximum tolerance decrease. Later text will further discuss this trimming capability.

If the resistor value shown on the schematic has a large tolerance, there may be no need for the design to allow for trimming. Thin film resistors can sometimes be fabricated to within $\pm 10\%$ tolerance without trimming. Thick film resistors can sometimes be fabricated to within $\pm 20\%$ tolerance. The manufacturing group should be consulted in such cases.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

The foregoing description of resistor design principles applies to any resistor design. When designing a particular resistor an important requirement is that the minimum allowable size for that particular resistor be established. Since space is usually at a premium, it is desirable to make the area (length and width) of the resistor as small as possible. However, one of two factors dictates the minimum allowable size of a particular resistor: the limitations of the manufacturing capability, or the thermal requirement that the resistor be of sufficient size to dissipate the heat generated when the resistor is functioning. The larger of the two has priority.

Manufacturing capabilities are called out in Tables 7.5.1-1 and 7.5.2-1.

The minimum size allowable for adequate wattage dissipation must be calculated. The procedure is as follows:

- 1) The maximum allowable wattage density must be established (i.e., the maximum wattage per square inch). 50 W/in^2 has often been used as a conservative rule-of-thumb for the allowable wattage density on alumina (Al_2O_3) substrates. On beryllia (BeO) substrates, 250 W/in^2 has been used. In metric units, these are: 0.077 W/mm^2 and 0.387 W/mm^2 , respectively.
- 2) The actual resistor wattage must be divided by the allowable wattage density in order to

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

2) (Cont.) determine the minimum area (square inches) that the resistor must provide in order to dissipate the heat. For example: If a one-quarter-watt resistor is to be integral with a substrate that can accept 50 watts per square inch, then the area of the resistor must be at least 0.005 in^2 (3.226 mm^2).

3) Knowing the minimum area, the allowable minimum width can be calculated using the following equation:

$$\text{Minimum Width} = \sqrt{\frac{(\text{Minimum Resistivity})(\text{Minimum Area})}{(\text{Final Value})}}$$

in which "Minimum Resistivity" is the nominal resistivity minus the resistivity tolerance.

4) The minimum length can be calculated as follows:

$$\text{Minimum Length} = \frac{\text{Minimum Area}}{\text{Minimum Width}}$$

The derivation of the minimum width equation is shown at the end of this section (7.8).

If the width needed for wattage is less than the trimming recommendation, then the larger width is used and the length will be increased to retain the same ratio to the new width as existed in the above calculation. Increasing these two dimensions will, of course, increase the area to greater than the minimum. This is not only acceptable; it is desirable.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Limits established by MIL-STD-883 prohibit any resistor width from being trimmed to less than 1 mil (0.0254 mm) for thin film, and 5 mils (0.127 mm) for thick film. For good yields in production quantities, more conservative figures are recommended: 5 mils and 10 mils (0.254), respectively. The calculation of the dimensions for trimming allowance will be discussed later. Thick and thin film resistors will be discussed separately.

The minimum width and length dimensions, calculated by the methods shown, assume a straight rectangular shape for the resistor. When the available space prohibits the resistor shape from being one straight bar (as shown in Figure 7.8-1), the bar can be folded back upon itself as many times as necessary. Such a shape is commonly referred to as "serpentine." When the shape becomes serpentine the previously calculated minimum width is still applicable but the length is not.

In a serpentine resistor, special consideration must be given to each corner (90° bend). The value of the resistance at each corner element has been empirically established as being approximately equivalent to $\frac{1}{2}$ of a square. This " $\frac{1}{2}$ square" is the commonly accepted value to be assigned to each corner element. (See Figure 7.8-2.)

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

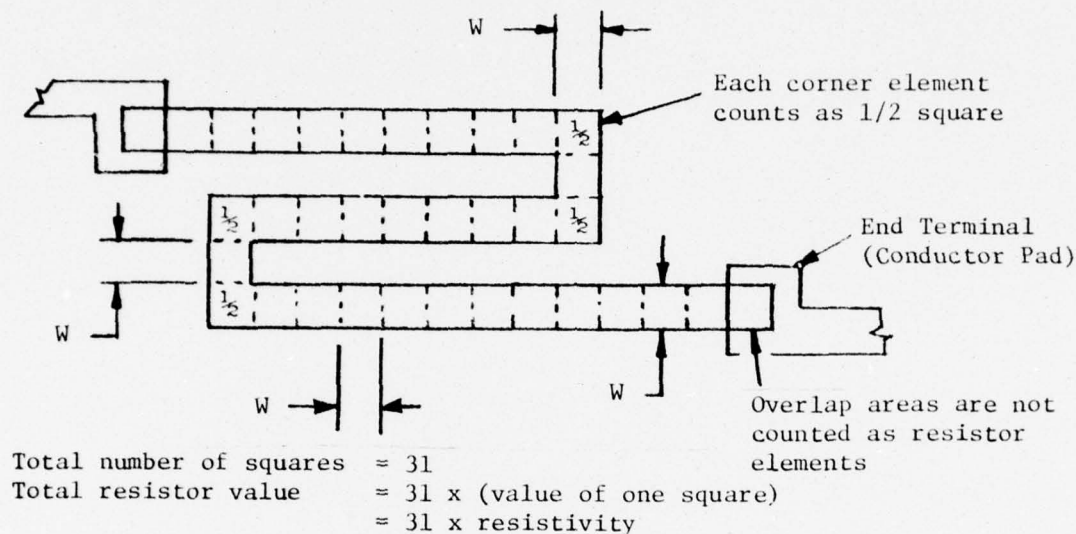
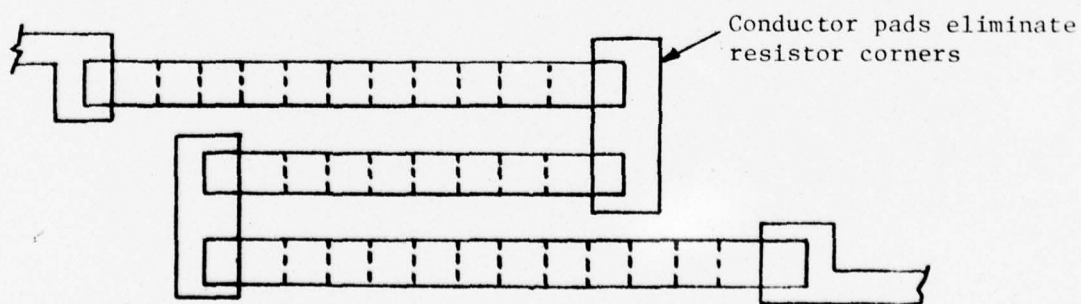


Figure 7.8-2 SERPENTINE RESISTOR

When high currents are required through the resistor, each sharp corner in a serpentine shape is a point that might experience high current density. If excessive current density is anticipated, the configuration shown in Figure 7.8-3 can be utilized.



Total number of squares $= 31$
 Total resistor value $= 31 \times (\text{value of each square})$
 $= 31 \times (\text{resistivity})$

Figure 7.8-3 SERPENTINE RESISTOR WITHOUT SHARP CORNERS

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Another generalization applicable to all resistors is that consideration should be given to the possibility of mask misalignment. Since the resistors and conductors are defined by separate masks, misalignment between masks is always a possibility. End terminals should be located 180° from each other (with respect to the resistor direction) in order that any mislocation of the resistor mask that affects the length of one end of the resistor will automatically be compensated by the opposite effect on the other end. Another way of expressing this guideline is that the resistor should always have an odd number of "legs."

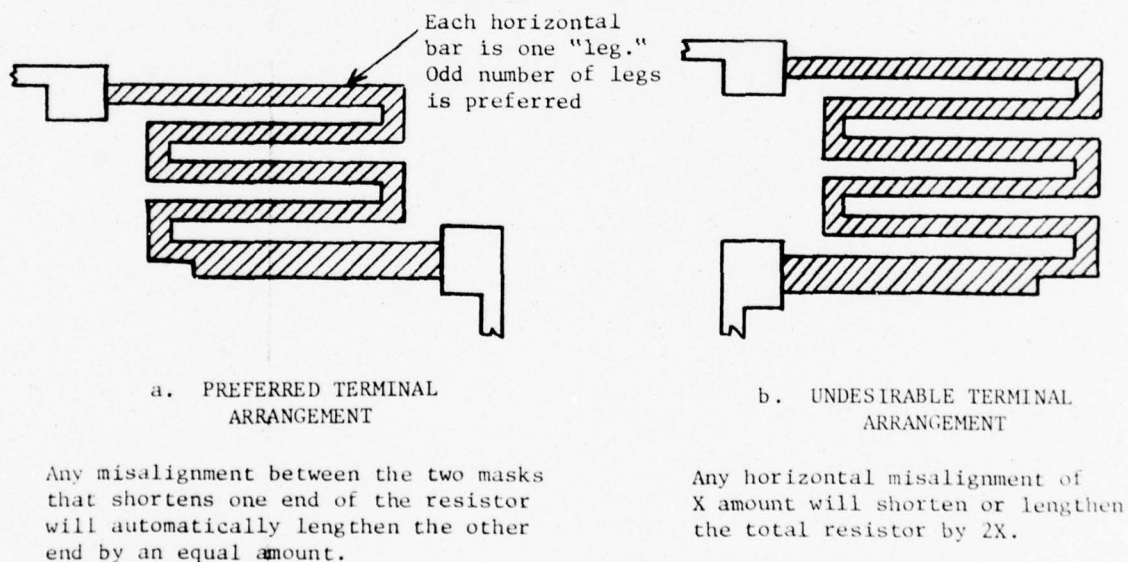
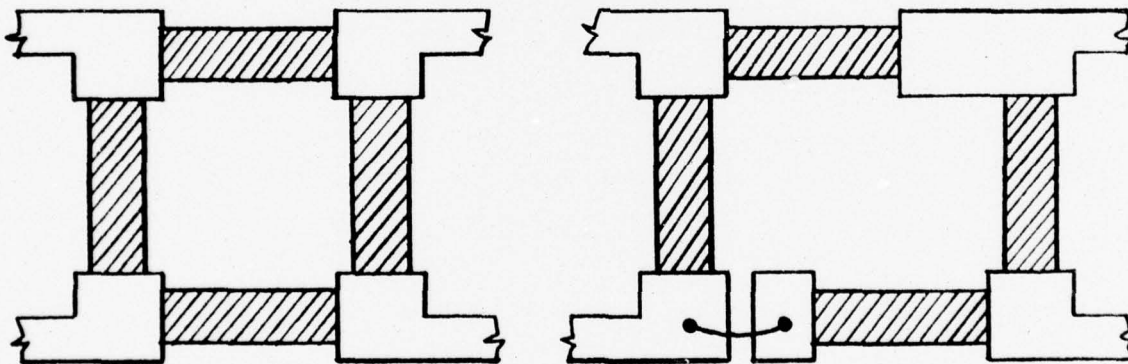


Figure 7.8-4 PREFERRED RELATIONSHIP OF RESISTOR END TERMINALS

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Any two resistors that require matching characteristics should be located as close to each other as possible so that the tolerances of each will be approximately equal.

Any group of resistors that is to be electrically connected in a closed loop cannot be fabricated as a closed loop. There must be a break somewhere in the loop to permit each resistor value to be measured and trimmed. During the wire-bonding operations, the break can be closed with a bonded wire.



WRONG

Closed resistor loop
cannot be trimmed.

RIGHT

Fabricated with break in loop.
Resistors measured and trimmed.
Loop closed with bonded wire.

Figure 7.8-5 CLOSED-LOOP RESISTOR GROUP

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

In summary, the procedure for the design of integral film resistors is as follows:

- 1) The resistivity of the resistor material must be established. For thin film resistors, this is specified by the manufacturing group. For thick film resistors, the layout designer selects the resistivity from a list of available values. (More discussion of guidelines for thick and thin film resistors will follow.)
- 2) The percentage of tolerance on resistivity must be specified by the manufacturing group.
- 3) The minimum size for fabrication and trimming must be established by the manufacturing group.
- 4) The minimum size allowable for heat dissipation must be calculated from the acceptable wattage density figure.
- 5) The shape and dimensions of the resistor are then determined, which will give the desired final value while meeting the following criteria:
 - a. The fabrication limitations have not been exceeded.
 - b. The minimum resistor width is not less than the minimum acceptable for trimming or wattage dissipation.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

5) (Cont.)

- c. The final resistor size (i.e., after trimming) will be sufficient to dissipate the maximum wattage.
- d. The maximum increase due to tolerance will not raise the pre-trimmed value beyond the desired final value.
- e. Sufficient trimming allowance has been made so that if the maximum decrease due to tolerance does occur, the resistor can be trimmed up to the desired final value.

The foregoing explanation is applicable to the design of either thick or thin film resistors. The decision to use one or the other must, of course, be made before the design begins and is often predicated upon the differences in the resistor performance characteristics. Thick film resistor values fluctuate more than thin film values. Some comparisons are shown below.

Temperature coefficients of resistance (TCR) for thick film resistors are generally from 50 to 250 ppm/ $^{\circ}\text{C}$. Some high resistivity pastes have TCRs of approximately 400 ppm/ $^{\circ}\text{C}$. Some thick film materials have negative TCRs in the low temperature range. Thin film TCRs can be expected to be between 50 and 100 ppm/ $^{\circ}\text{C}$. And these TCRs are all positive. (A 2.7k Ω resistor having a TCR of 50 ppm/ $^{\circ}\text{C}$ will vary 0.135 Ω per each $^{\circ}\text{C}$ temperature change.)

After being subjected to 150 $^{\circ}\text{C}$ for 1,000 hr, thick film resistor values may vary from 0.5% to 3%. Thin film values can be expected to remain within 0.01 to 0.1% of their original value.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Whether for thick or thin film, it is recommended that all the resistors required for a particular substrate layout be designed before beginning the layout.

The next two sections, 7.8.1 and 7.8.2, will show examples of thick and thin film resistor designs using specific values.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

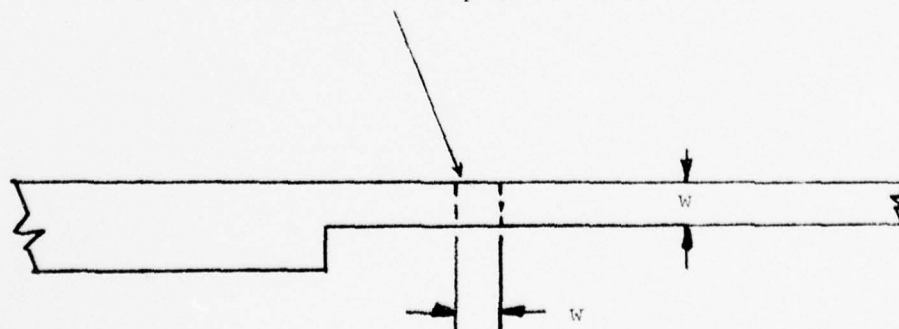
Derivation of Equation for Determining Minimum Resistor Width.

Since the same current flows through the entire length of the resistor, the risk of a hot-spot occurs in the narrowest portion of the resistor. "Hot-spot" is defined as any incremental area within which the allowable wattage density is exceeded.

In order to specify the minimum width acceptable to provide adequate wattage dissipation, an algebraic equation must be available which expresses the actual wattage density within the smallest incremental area; and that wattage density must be expressed as a function of the width of that incremental area. Then, by setting that actual wattage density equal to the allowable wattage density, the equation could be solved for the width.

Given: An incremental square area within the narrowest portion of the resistor, having a width of w , and an allowable wattage density designated APD.

The incremental square can be any square within the narrowest part of the resistor.



7.8 (Cont.) INTEGRAL RESISTOR DESIGN

Call the actual wattage dissipated within the incremental square P_{\square} .

Call the wattage density of the incremental square PD_{\square} .

$$PD_{\square} = \frac{P_{\square}}{\text{Area of Incremental Square}} = \frac{P_{\square}}{w^2} \quad (1)$$

$$P_{\square} = (I)^2 R_{\square} \quad (2)$$

where I is the current through the resistor, and R_{\square} is the resistance value of the incremental square.

To make P_{\square} maximum, R_{\square} must be minimum. (I increases as R_{\square} decreases. But with respect to P_{\square} , I increases as the square, whereas R_{\square} decreases linearly.)

Since the resistance of the incremental square (R_{\square}) is numerically equal to the minimum resistivity (abbreviate as "Min Rstv" ^{L1}), then substituting into equation (2) gives:

$$P_{\square} = (I)^2 (\text{Min Rstv})(l_{\square}) \quad (3)$$

We can express I^2 in terms of the schematic values:

$$(I)^2 = \frac{\text{Total Resistor Wattage}}{\text{Resistor Value}} \quad (4)$$

^{L1} Min Rstv is the rated resistivity minus the resistivity tolerance.

7.8 (Cont.) INTEGRAL RESISTOR DESIGN

For the sake of brevity, call Total Resistor Wattage "Total Wattage". Call Resistor Value "Final Value" to distinguish from the value before trimming.

$$P_{\square} = \frac{(\text{Total Wattage}) (\text{Min Rstv}) (1 \square)}{\text{Final Value}} \quad (5)$$

$$PD_{\square} = \frac{(\text{Total Wattage}) (\text{Min Rstv})}{(\text{Final Value}) (w)^2} \quad (6)$$

We can assure that PD_{\square} will not exceed the allowable wattage density by setting PD_{\square} equal to the allowable wattage density; abbreviate as "APD." Thus, equation (7).

$$APD = \frac{(\text{Total Wattage}) (\text{Min Rstv})}{(\text{Final Value}) (w)^2} \quad (7)$$

Solving for $(w)^2$ gives:

$$(w)^2 = \frac{(\text{Total Wattage}) (\text{Min Rstv})}{(\text{Final Value}) (APD)} \quad (8)$$

$$w = \sqrt{\frac{(\text{Total Wattage}) (\text{Min Rstv})}{(\text{Final Value}) (APD)}} \quad (9)$$

However, $\frac{\text{Total Wattage}}{APD}$ is equal to the Minimum Area. Therefore

$$\text{Minimum Width} = \sqrt{\frac{(\text{Min Rstv}) (\text{Min Area})}{(\text{Final Value})}} \quad (10)$$

Either of equations (9) or (10) can be used to determine the minimum width.

7.8.1 Thick Film Resistor Design

This section will show, by specific examples, the design of thick film resistors in accordance with the guidelines described in the preceding section.

The resistivity of the thick film material must be selected (usually by the layout designer) to suit each resistor. More than one material can be used on one substrate. However, it is always a design goal to minimize the variety of material resistivities on one substrate. Each resistivity requires a separate mask and must be separately processed.

The commonly used resistivities of thick film material are:

10 Ω/\square	5 $k\Omega/\square$
100 Ω/\square	10 $k\Omega/\square$
500 Ω/\square	100 $k\Omega/\square$
1 $k\Omega/\square$	1 $M\Omega/\square$

The usual tolerance on thick film resistivity can be expected to be between 20% and 30%. The manufacturing group should specify the actual tolerance to be applied for each type of paste.

The following is an example of resistor designs for one substrate.

Given that the substrate can dissipate 50 W/in² (0.775 W/mm²) that the resistivity tolerance is to be $\pm 25\%$, and that the circuit schematic calls for the following resistor values:

7.8.1 (Cont.) Thick Film Resistor Design

REF. DESIG.	SCHEMATIC CALLOUTS		
	VALUE (Ω)	TOLERANCE (%)	POWER (W)
R1	2.7 k	10	0.25
R2, 3	10 k	5	0.05
R4	47 k	5	0.10
R5	2.7 k	10	0.50
R6	1 k	10	0.10

Listing the data in chart form, as shown, can be an advantage. As the design proceeds, additional columns can be added to the chart, as shown in Table 7.8.1-1. The total resistor design data can be presented in this efficient, graphic manner. The tolerance shown is not the tolerance that must be compensated by trimming. It is the accuracy of the final resistor value. Including such information in the chart allows the chart to be used in establishing the parameters for the trimming accuracy.

The selection of the material resistivity is made by judgment. For all resistors except R4, use $1 \text{ k } \Omega/\square$. Using $1 \text{ k } \Omega/\square$ for R4 would require a large number of squares causing the length to be too long (>1.00 inch). For R4, either 10 or $100 \text{ k } \Omega/\square$ would be acceptable. Presume an arbitrary choice of the $10 \text{ k } \Omega/\square$.

The minimum area of each resistor can next be added to the chart. Remember that this is the minimum area required when the resistor is functioning in the electrical circuit. Translated into the processing sequences, it means minimum area "after trimming."

7.8.1 (Cont.) Thick Film Resistor Design

Table 7.8.1-1 EXAMPLE OF RESISTOR DESIGN DATA CHART

REF. DESIG.	SCHEMATIC CALLOUTS			MAT'L. RSTV. (Ω/\square)	MIN. AREA in. ² (mm ²)	MIN. WIDTH		DESIGN VALUE (Ω)	LENGTH		WIDTH	
	VALUE (Ω)	TOL. (%)	POWER (Watts)			in.	(mm)		in.	(mm)	in.	(mm)
R1	2.7 k	10	0.25	1 k								
R2, 3	10 k	5	0.05	1 k								
R4	47 k	5	0.10	10 k								
R5	2.7 k	10	0.50	1 k								
R6	1 k	10	0.10	1 k								

7.8.1 (Cont.) Thick Film Resistor Design

Using R4 as a sample:

$$\frac{0.10 \text{ W}}{50 \text{ W/in.}^2} = 0.002 \text{ in.}^2$$

REF. DESIG.	MIN. AREA	
	in ²	(mm ²)
R1	0.005	(3.226)
R2, 3	0.001	(0.645)
R4	0.002	(1.290)
R5	0.010	(6.452)
R6	0.002	(1.290)

Knowing the resistivity tolerance and the minimum area after trimming, and having selected the resistivity, the minimum dimensions allowable after maximum trimming can be determined.

$$\text{Minimum Width} = \sqrt{\frac{(\text{Min. Resist.}) (\text{Min. Area})}{\text{Final Value}}}$$

$$\text{Minimum Length} = \frac{\text{Min. Area}}{\text{Min. Width}}$$

Using R1 as a sample:

$$\text{Minimum Width} = \frac{(750 \Omega/\square)(0.005 \text{ in.}^2)}{2700 \Omega} = 0.0373 \text{ in. (0.947 mm)}$$

$$\text{Minimum Length} = \frac{0.005 \text{ in.}^2}{0.0373 \text{ in.}} = 0.1340 \text{ in (3.404 mm)}$$

This information should be added to the resistor data chart to serve as inspection criteria.

7.8.1 (Cont.) Thick Film Resistor Design

If the width is reduced to less than the calculated minimum, because of trimming or any other reason, then the potential for a hot-spot exists and the reliability of the part is compromised.

REF. DESIG.	MIN. WIDTH in. (mm)	LENGTH in. (mm)
R1	0.0373 (0.947)	0.1340 (3.404)
R2, 3	L^1	L^1
R4	0.0178 (0.452)	0.1123 (2.852)
R5	0.0527 (1.339)	0.1897 (4.818)
R6	0.0387 (0.983)	0.0517 (1.313)

L^1 For R2, 3 the minimum width calculated to be 0.0087 (0.221 mm); the length 0.1149 (2.918 mm). Since this minimum width needed for wattage is less than the recommended 0.010 (0.254 mm) minimum for trimming, the larger requirement has priority. Increase the minimum width to 0.010. Since the previous ratio of length to width was 13.2 to one, this ratio must remain for the new length. The new length is 0.132.

Using the 25% resistivity tolerance, the design value (value before trimming, often called the "as-fired" value) of each resistor can be calculated. The design value can be calculated either of two ways.

7.8.1 (Cont.) Thick Film Resistor Design

One way is such that the total value after maximum tolerance increase will equal the desired schematic value:

$$(\text{Design Value}) + (\text{Maximum Tolerance Increase}) = \text{Schematic Value}$$

$$(\text{Design Value}) + 25\% (\text{Design Value}) = \text{Schematic Value}$$

$$1.25 (\text{Design Value}) = \text{Schematic Value}$$

$$\text{Design Value} = \frac{\text{Schematic Value}}{1.25}$$

The other way is to insure that the total value after maximum increase will be less than the desired schematic value. This is a rule-of-thumb calculation; it subtracts the tolerance directly from the schematic value.

$$(\text{Design Value}) = (\text{Schematic Value}) - (\text{Rstv. Tolerance})(\text{Schematic Value})$$

$$\text{Design Value} = (\text{Schematic Value}) - 25\% (\text{Schematic Value})$$

$$\text{Design Value} = 0.75 (\text{Schematic Value})$$

The second method applied to the sample resistors gives:

7.8.1 (Cont.) Thick Film Resistor Design

REF. DESIG.		DESIGN VALUE (Ω)
R1		2.025 k
R2, 3		7.5 k
R4		35.25 k
R5		2.025 k
R6		0.75 k

Applying a 25% increase to any of the values shown verifies that even with the increase, the as-fired value will still be less than the desired schematic value.

$$\text{Sample: } 2.025 \text{ k}\Omega + 25\% (2.025 \text{ k}\Omega) = 2.531 \text{ k}\Omega$$

Having the design value determined, the number of squares before trimming can now be determined for each resistor, using the nominal value of resistivity.

$$\frac{\text{Design Value}}{\text{Resistivity}} = \text{Number of squares required before trimming.}$$

$$\text{Using R1 as a sample: } \frac{2.025 \text{ k}\Omega}{1 \text{ k}\Omega/\square} = 2.025 \text{ squares}$$

Now the ratio of the length to the width is known (the number of squares is the number of "widths"); and since the length before trimming is the same length already calculated for minimum length,

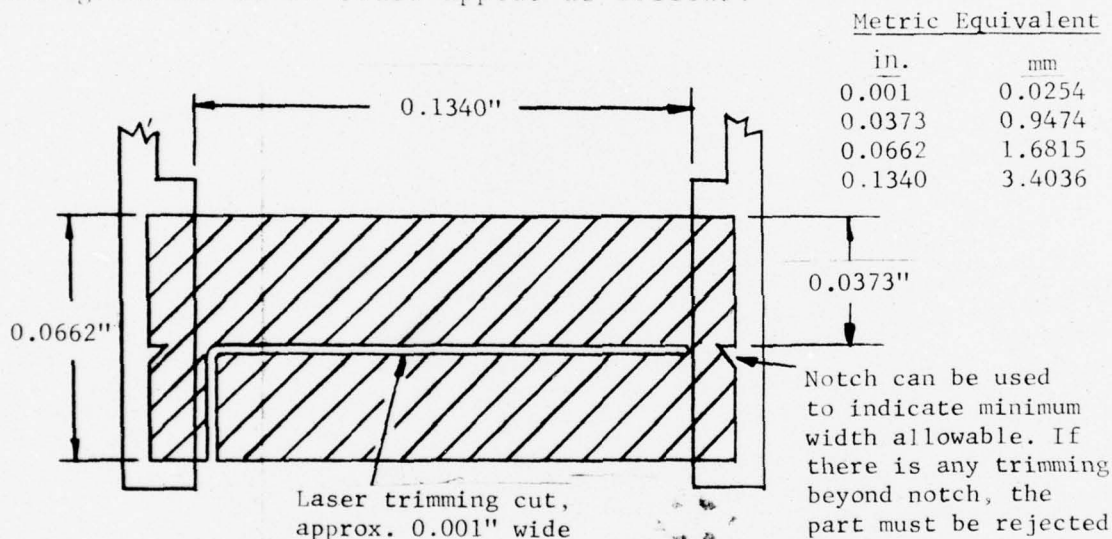
7.8.1 (Cont.) Thick Film Resistor Design

the width before trimming is:

$$\text{Design Width} = \frac{\text{Length}}{\text{Number of Squares}}$$

Using R1 as a sample: $\text{Width} = \frac{.1340}{2.025} = 0.0662 \text{ (1.681 mm)}$

Assuming that maximum trimming is required, the final physical configuration of R1 could appear as follows:



It is not to be inferred from the above sketch that the trimming cut and dimensions are to be depicted on the layout. The design length and width should be drawn as accurately as practical; but the exact dimensions will appear in the chart.

If the available layout space permits, the design length and width can be increased in order to have the layout lines lie on a full grid or half-grid position. The width can also be increased beyond its ratio to the length. This would mean fewer squares and a lower value before trimming, but the minimum allowable width

7.8.1 (Cont.) Thick Film Resistor Design

(0.0373) would be unchanged. Using R1 as an example, a length of 0.135 and width of 0.0675 would be on half-grid at 20 x scale; these changes would cause the length to be exactly two squares long instead of 2.025. This would be perfectly acceptable, because this lower design value can still be trimmed up to the desired final value.

After calculating the width for each resistor, the chart will be as shown in Table 7.8.1-2.

Except for R2, 3, all the resistor dimensions were dictated by the wattage dissipation. Because R2, 3 were adjusted to larger-than-minimum required for wattage, a new factor should be considered in the trimming requirements. The previous calculation has already established that if the resistivity is minimum, the ratio of length to width is 13.2 after trimming.

Using the new design length of 0.225 (as explained in footnote) and maintaining the previous 13.2 ratio required after trimming, gives a new width-after-trimming of 0.017 (0.432 mm). This dimension can be designated as a sufficient trim dimension. The sufficient-trim-dimension is that dimension sufficient to accommodate the maximum amount of trimming. 0.0087 (0.221 mm), the previously calculated minimum width to avoid hot-spots is still applicable.

It is recommended that some cross-reference symbol be put in the "Min. Width" column of the chart, and a note appear on the layout explaining that 0.0087 is absolute minimum and that 0.017 is sufficient. The manufacturing group might choose to trim to 0.010 in which case trimming would not be required along the full length.

7.8.1 (Cont.) Thick Film Resistor Design

Table 7.8.1-2 COMPLETED RESISTOR DATA CHART

REF. DESIG.	SCHEMATIC CALLOUTS	TOL. (%)	POWER (WATTS)	NAT'L RSTV (Ω/\square)	MIN. AREA in. ² (mm ²)	MIN. WIDTH in. (mm)	DESIGN VALUE (Ω)	LENGTH in. (mm)	WIDTH in. (mm)
R1 ¹	2.7 k	10	0.25	1 k	0.005 (3.226)	0.0373 (0.947)	2.025 k	0.1340 (3.404)	0.0662 (1.681)
R2, 3	10 k	5	0.05	1 k	0.001 (0.645)	L^3	7.5 k	L^2	L^2
R4	47 k	5	0.10	10 k	0.002 (1.290)	0.0178 (0.452)	35.25 k	0.1123 (2.852)	0.0318 (0.808)
R5 ²	2.7 k	10	0.50	1 k	0.010 (6.452)	0.0527 (1.339)	2.025 k	0.1897 (4.818)	0.0937 (2.380)
R6	1 k	10	0.10	1 k	0.002 (1.290)	0.0387 (0.983)	0.75 k	0.0517 (1.313)	0.0689 (1.750)
RESISTIVITY TOLERANCE = \pm 25%									

¹ While R1 and R5 require the same final value and use the same resistivity, their dimensions vary because the wattage requirements vary.

² R2, 3 were the only resistors for which the calculated design width was less than the 0.030 (0.447 mm) recommended for fabrication. Therefore increase the width to 0.030. Maintaining the number of squares at 7.5, gives a new length of 0.225 (5.715 mm).

³ See text description of sufficient-trim-dimension.

7.8.1 (Cont.) Thick Film Resistor Design

Any trimming beyond the 0.0087 dimension is cause for rejecting the part.

If maximum trimming is required, then the trimming of R2 and R5 could be one of the configurations shown in Figure 7.8.1-1.

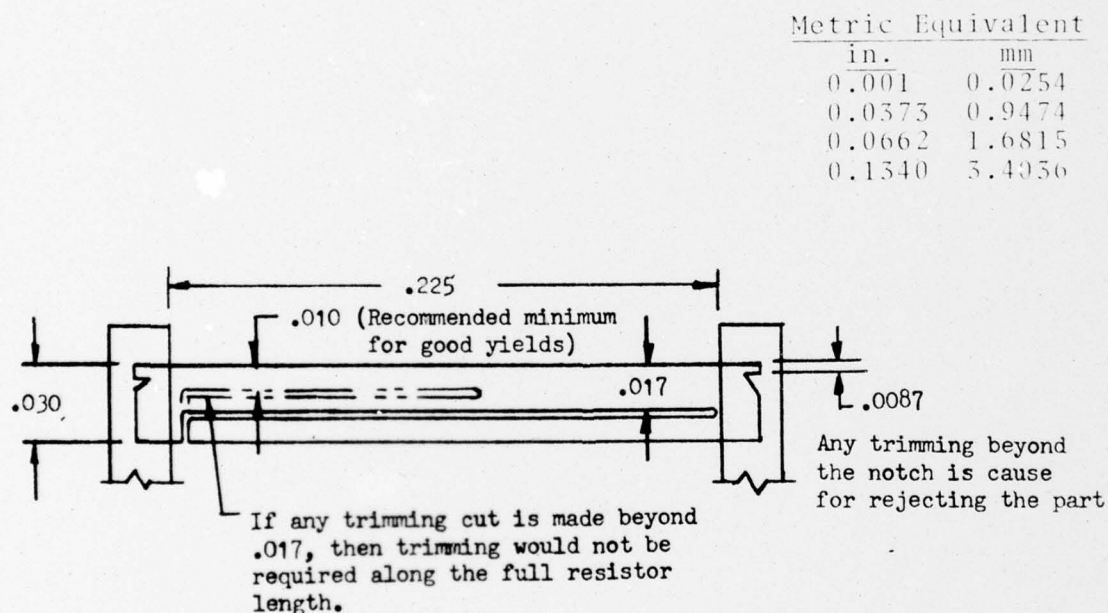


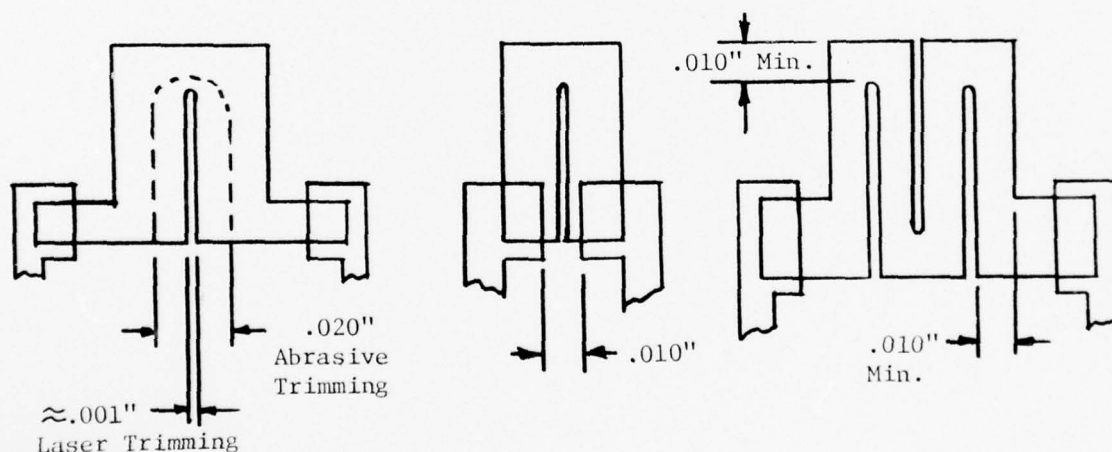
Figure 7.8.1-1 ALTERNATIVE TRIMMING CONFIGURATIONS

In the foregoing examples, each resistor was designed to 75% of the desired final value. If the maximum tolerance increase (25%) occurs before trimming each resistor will be 93.75% of its final value. For R1, R5, and R6 there would be no need for trimming because each would be within the 10% accuracy required for final value. R2, 3, 4, and 5 would still need to be trimmed.

7.8.1 (Cont.) Thick Film Resistor Design

When programmable automatic trimming equipment is being used, the entire trimming operation is so fast that having to trim or not trim a few individual resistors is of almost no consequence. However, when the trimming is performed with manually operated equipment, each operation adds significantly to the manufacturing time. Therefore, when manual equipment is to be used, the more precise method of computing the design value should be used, which might eliminate the need to trim some resistors. In the discussion of thin film resistor design (Section 7.8.2) the more precise method will be demonstrated.

There are several noteworthy resistor configurations known as "top-hats." Figure 7.8.1-3 shows some examples.



Metric Equivalent

<u>in</u>	<u>mm</u>
.001	0.025
.010	0.254
.020	0.508

Figure 7.8.1-3 TOP-HAT RESISTOR CONFIGURATIONS

7.8.1 (Cont.) Thick Film Resistor Design

By using top-hat configurations, serpentine shapes can be achieved within less space. Top-hats also provide the capability to trim the resistance from a very low value to a high value. This capability can allow one basic substrate configuration to be used in various applications requiring a wide range of resistor values.

Material manufacturers recommend that resistors using high-resistivity pastes have longer minimum lengths, because these pastes reach their rated resistivities only at or above certain minimum lengths. Figure 7.8.1-3 shows the characteristics of one manufacturer's $10 \text{ M}\Omega/\square$ paste.

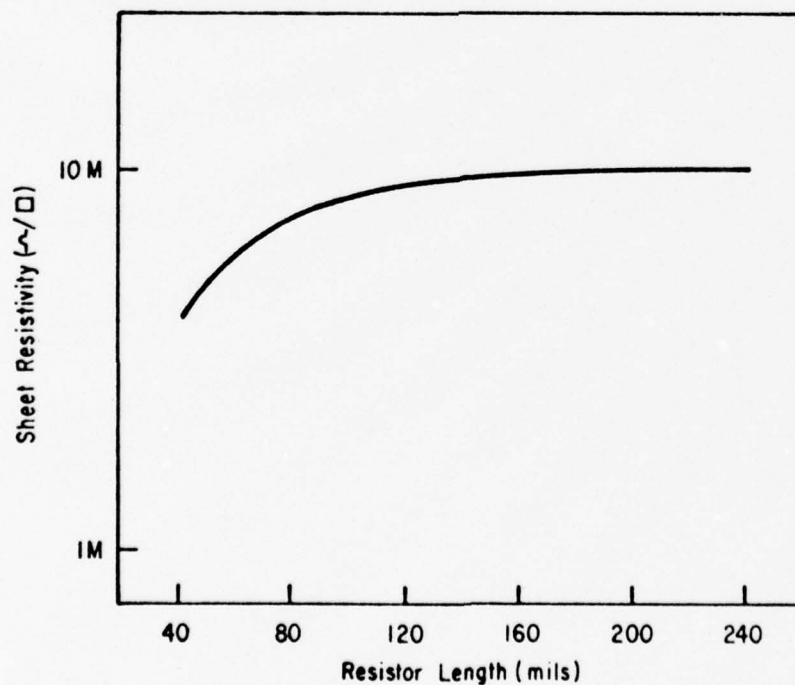


Figure 7.8.1-3 SHEET RESISTIVITY VS. RESISTOR LENGTH

7.8.1 (Cont.) Thick Film Resistor Design

The graph indicates that this particular material is only $6 \text{ M } \Omega/\square$ for a resistor length of 40 mils. And that the rated value of $10 \text{ M } \Omega/\square$ applies only for resistor lengths of 180 mils or longer.

7.8.2 Thin Film Resistor Design

This section will demonstrate the design of thin film resistors in accordance with the guidelines shown in Section 7.8.

A thin film resistor is usually designed to have one of two typical shapes: either a rectangular bar or a serpentine shape. Either of these may have a "trim-bar" area (Figure 7.8.2-1).

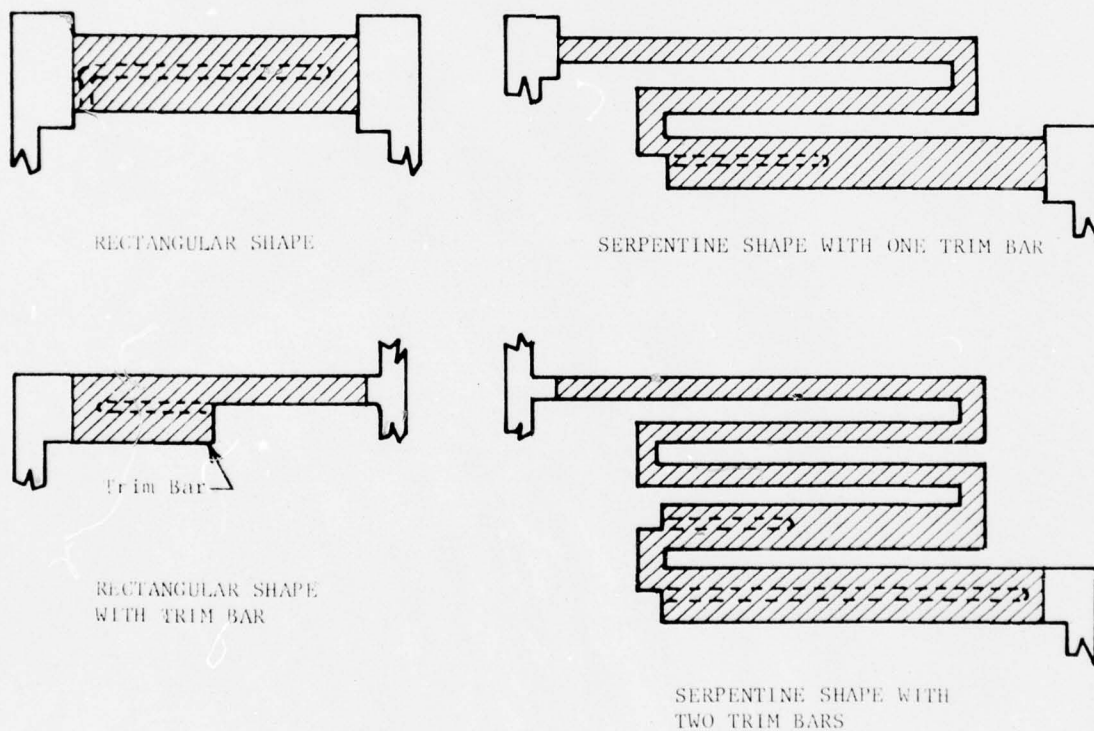


Figure 7.8.2-1 EXAMPLES OF TYPICAL THIN FILM RESISTOR SHAPES

It is recommended that the resistors required for a particular substrate layout be designed before beginning the layout.

7.8.2 (Cont.) Thin Film Resistor Design

The resistivity of a thin film resistor is typically within the range from $25 \Omega/\square$ to $1,000 \Omega/\square$ depending upon the composition and thickness of the material used.

The most commonly used material is nickel chromium (usually referred to as "nichrome"). The examples shown in this section will presume $100 \Omega/\square$ (a commonly used resistivity value of nichrome).

It is not unusual for thin film resistors to be processed to within 10% tolerance; however, the example herein will presume a conservative $\pm 20\%$ resistivity tolerance. This means that the resistivity could be in the range from $80 \Omega/\square$ to $120 \Omega/\square$.

The minimum resistor widths must be 5 mils (0.127 mm) in areas where no trimming will be done; 12.5 mils (0.317 mm) in trimming areas.

For the example, assume an allowable wattage density (APD) of 25 W/in.^2 (0.0387 W/mm^2). Assume resistor values as shown below:

REF. DESIG.	SCHEMATIC CALLOUTS			
	VALUE (Ω)	TOL. (%)	POWER (Watts)	
R1	2.7k	5	0.10	
R2, 3	1k	5	0.25	
R4	100	1	0.25	
R5	4.7k	1	0.10	
R6	10k	5	0.05	

7.8.2 (Cont.) Thin Film Resistor Design

Calculation of the minimum acceptable area proceeds as follows:

$$\frac{\text{Actual Wattage}}{\text{Allowable Wattage Density}} = \text{Minimum Area}$$

Using R1 as a sample: $\frac{0.10W}{25 W/in.^2} = .004 in.^2 (2.584 mm^2)$

This means that R1 must be at least 0.004 in.² after maximum trimming.

Continuing the calculations for the remaining resistors gives:

REF DESIG.	MIN. AREA	
	(in. ²)	(mm ²)
R1	0.004	(2.580)
R2,3	0.010	(6.452)
R4	0.010	(6.452)
R5	0.004	(2.580)
R6	0.002	(1.290)

The minimum width required to avoid hot-spots needs to be determined.

$$\text{Min. Width} = \sqrt{\frac{(\text{Min. Area}) (\text{Min. Rstv.}) (1 \square)}{\text{Final Value}}}$$

Using R1 as a sample:

$$\text{Min. Width} = \sqrt{\frac{(0.004 in.^2) (80 \Omega/\square)}{(2700 \Omega)}} = 0.0109 in. (0.277 mm)$$

$$\text{The minimum length is } L = \frac{\text{Min. Area}}{\text{Min. Width}}$$

$$\text{For R1: } L = \frac{0.004 in.^2}{0.0109 in.} = 0.3670 in. (9.322 mm)$$

7.8.2 (Cont.) Thin Film Resistor Design

Repeating the calculations for each resistor gives:

REF. DESIG.	MIN. WIDTH	LENGTH
	in. (mm)	in. (mm)
R1	0.0109 (0.277)	0.3670 (9.322)
R2,3	0.0283 (0.719)	0.3533 (8.974)
R4	0.0894 (2.271)	0.1118 (2.840)
R5	0.0082 (0.208)	0.4878 (12.390)
R6	L^1	L^1

L^1 R6 is the only case for which the calculated minimum width was less than the 5 mil (0.127 mm) minimum recommended for good yields in the trimming operation. (R6 calculated to a 4 mil (0.102 mm) width and 500 mil (12.70 mm) length). Increase the width to 5 mils. Now maintaining the ratio of 125 between length and width gives a new length of 625 mils (15.88 mm). Presuming that such a long resistor will be difficult to accommodate within the substrate layout, a serpentine shape should be designed.

The dimensions calculated for the resistors are the minimum dimensions required to dissipate heat. They are the minimum dimensions required after trimming, which means that these dimensions apply to the resistors when they are at their final resistance values. Prior to trimming, the resistors are at a lower value (in this text called "design value"). Before designing the serpentine shape, the design value needs to be determined because this is the value of the serpentine resistor prior to trimming.

The design values (values before trimming) will be calculated using the method that gives the exact final value when maximum tolerance increase occurs.

$$\text{Design Value} = \frac{(\text{Final Value})}{1.20}$$

For R1 this becomes 2.250 k Ω .

7.8.2 (Cont.) Thin Film Resistor Design

The design values for all the resistors are as follows:

REF. DESIG.		DESIGN VALUE (Ω)
R1		2.250k
R2,3		0.833k
R4		83.333
R5		3.916k
R6		8.333k

NOTE: To calculate design values that would remain less than the desired final value after maximum tolerance increase, a rule-of-thumb method can be used:

$$\text{Design Value} = (\text{Final Value}) (1 - \text{Rstv. Tolerance})$$

It will be convenient in the design of the serpentine shape to use the number-of-squares in each resistor. Dividing the design value by the value per square (i.e., nominal resistivity) gives the number of squares required.

$$\frac{\text{Design Value}}{\text{Resistivity}} = \text{Number of Squares Required}$$

$$\text{Using R1 as a sample: } \frac{2250 \Omega}{100 \Omega/\square} = 22.5 \text{ squares}$$

This means that before trimming the length of R1 will be equal to 22.5 squares.

7.8.2 (Cont.) Thin Film Resistor Design

The remaining resistors are:

R2, 3	=	8.333 squares
R4	=	0.833 squares
R5	=	39.166 squares
R6	=	83.333 squares

In a rectangular shape, the trimming can easily be performed along the full length of the resistor. In a serpentine shape it would be very difficult, if not impossible, to trim continuously throughout the full length. Therefore, if at all possible, the trim bar should be on only one leg of the serpentine resistor. The equation expressing the minimum required trimming length is:

$$\text{Min. Trim Length} = \frac{(\text{Final value}) - (1 - \text{Rstv. Tolerance})(\text{Design value})}{\frac{(\text{Min. Rstv.})}{(\text{Width after trim})} - \frac{(\text{Min. Rstv.})}{(\text{Width before trim})}}$$

The derivation of the above equation is given at the end of this section.

Remembering that the width after trimming is 5 mils (0.127 mm), and before trimming is 12.5 mils (0.317 mm), now apply the formula to R6 (call minimum trimming length (L_t)):

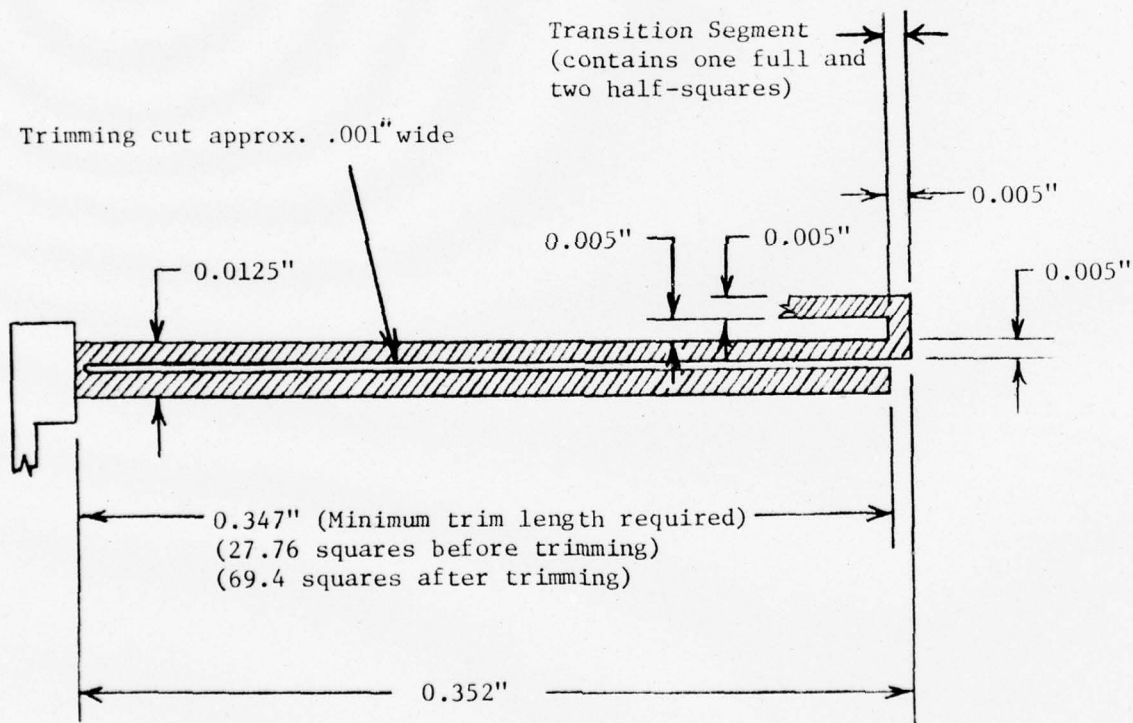
$$L_t = \frac{(10,000 \Omega) - (1 - 0.20)(8,333 \Omega)}{\frac{80 \Omega / \square}{0.005 \text{ in.}} - \frac{80 \Omega / \square}{0.0125 \text{ in.}}} = 0.347 \text{ in. (8.814 mm)}$$

347 mils is the minimum length of trim bar, having a resistivity of $80 \Omega / \square$ that when trimmed from a width of 12.5 mils to a width of 5 mils will raise its value by 3333.33Ω . This 3333.33Ω is the amount the resistor would need to be raised from its lowest value of $6,666.66 \Omega$ (due to tolerance) to the final value of $10,000 \Omega$.

7.8.2 (Cont.) Thin Film Resistor Design

Assuming that this length is not too long for the layout, the trimming can be accomplished on only one leg of the resistor.

The one leg where trimming will be performed looks thus:



Metric Equivalents

in.	mm
0.005	0.127
0.125	0.317
0.347	8.81
0.352	8.94

Figure 7.8.2-2 TRIM BAR DIMENSIONS

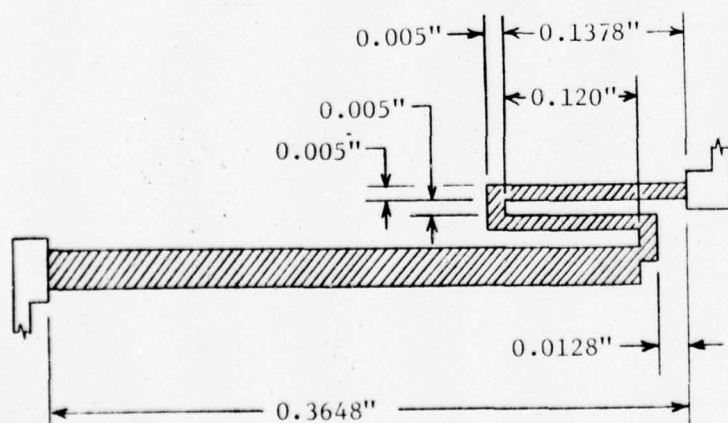
7.8.2 (Cont.) Thin Film Resistor Design

NOTE: If the 0.347 in. leg length is too long for the space available on the layout, then the 0.347 minimum trimming length can be divided between two legs, each one shorter than 0.347, but not necessarily equal to each other.

The design of the remaining portion of the resistor proceeds as follows. The trim bar plus the transition segment shown in Figure 7.8.2-2 contain a total of 29.76 squares. The total squares required for design value is 83.333, so the rest of the resistor will need to contain 53.573 squares. Because an odd number of legs is always a design goal, arbitrarily choose three legs. Since two squares (one full and two halves) will be provided by the transition segment between the second and third legs, only 51.573 squares will need to be provided by the two remaining legs. The third leg needs to be approximately 10 mils (0.254 mm) beyond the first transition segment in order to accommodate the end terminal. This means the third leg should be approximately .015" (i.e., three squares) longer than the second. Divide the 51.573 squares into 24 squares for the second leg and 27.573 for the third. Use 0.005" as the width of each of the two legs.

24 squares @ 0.005" each = 0.120"

27.573 squares @ 0.005" each = 0.1378"



Metric Equivalent

in	mm
0.005	0.127
0.0128	0.325
0.120	3.048
0.1378	3.50
0.3648	9.27

The trim cut need not be shown on the design layout; but sufficient dimensions do need to be shown to completely define the resistor.

7.8.2 (Cont.) Thin Film Resistor Design

If the resistivity is minimum ($80\Omega/\square$), the trimming cut will be made continuous through the full length of the trim bar and the total number of squares will be 124.973. At $80\Omega/\square$ the total resistance will be 9997.84Ω . If the resistivity were maximum ($120\Omega/\square$), the total value before trimming would be 9999.96Ω . No trimming would be required.

Each of the other resistors will presumably have rectangular shapes. Their design widths can be calculated as follows:

$$\text{Design Width} = \frac{\text{Length}}{\text{Number of Squares}}$$

Using R1 as a sample:

$$\text{Design Width} = \frac{0.3670''}{22.5} = 0.0163'' (0.414 \text{ mm})$$

7.8.2 (Cont.) Thin Film Resistor Design

The complete resistor data chart is shown in Table 7.8.2-1.

Table 7.8.2-1 COMPLETED RESISTOR DATA CHART

REF DESIG.	SCHEMATIC CALLOUTS			MIN. AREA in. 2 (mm ²)	MIN. WIDTH in. (mm)	DESIGN VALUE (Ω)	LENGTH		WIDTH	
	VALUE (Ω)	TOL. (%)	POWER (Watts)				in. (mm)	in. (mm)		
R1	2.7 k	5	0.10	0.004 (2.581)	0.0109 (0.277)	2.250 k	0.3670 (9.322)	0.0163 (0.414)		
R2, 3	1.0 k	5	0.25	0.010 (6.452)	0.0283 (0.719)	0.833 k	0.3533 (8.974)	0.0424 (1.077)		
R4	100	1	0.25	0.010 (6.452)	0.0894 (2.271)	83.333	0.1118 (2.840)	0.1342 (3.409)		
R5	4.7 k	1	0.10	0.004 (2.581)	0.0082 (0.208)	3.916 k	0.4878 (12.390)	0.0125 (0.317)		
R6	10 k	5	0.05	0.002 (1.290)	0.0040 (0.1016)	8.333 k	SERPENTINE			
RESISTIVITY = 100 Ω/□ , ± 20%										

7.8.2 (Cont.) Thin Film Resistor Design

NOTE: Each of the resistors meets the fabrication and trimming requirements. For R6, the Min. Width is shown as 0.004". Any trimming beyond this dimension should be cause for rejection, since a potential hot spot would exist. The trimming should be performed at the 0.005"-width in order to achieve better yields.

It is acceptable to increase the dimensions so that the layout lines will fall on a full-grid or half-grid increment, provided the value remains within the acceptable range. The minimum width (to avoid hot spots) will not change.

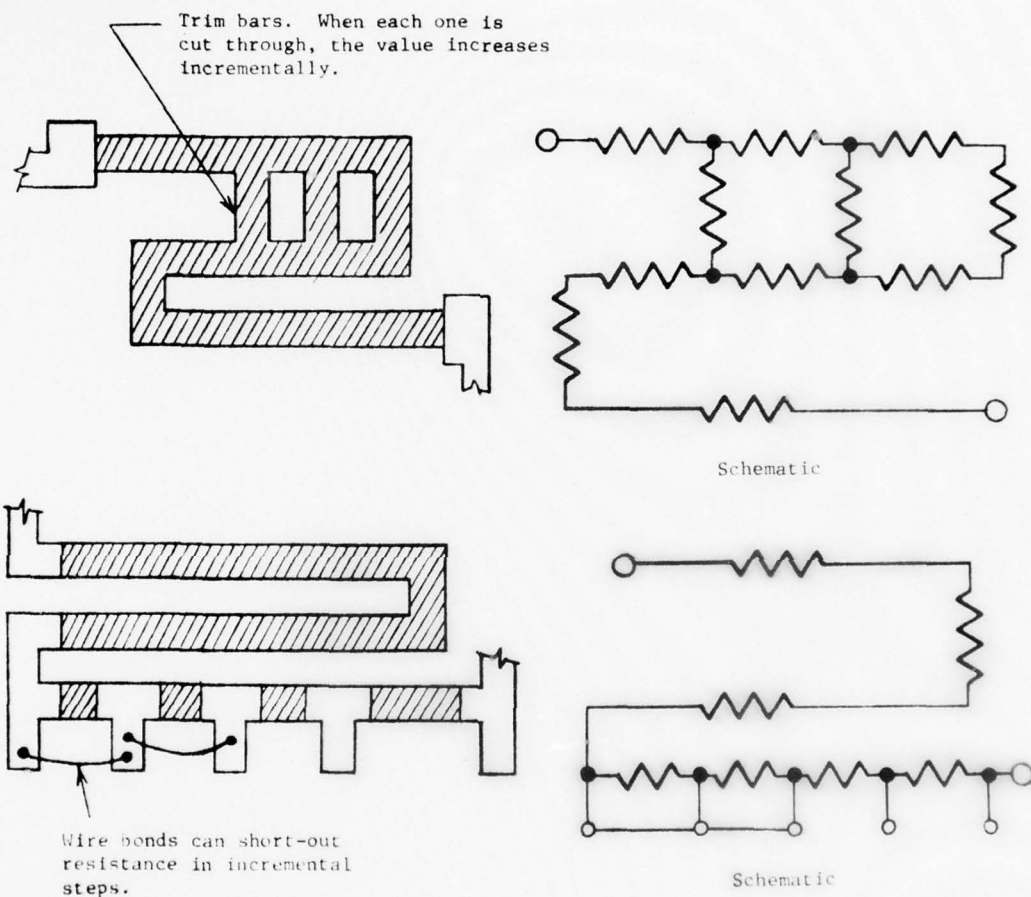
Example. If R4 changes to 0.1125 in. (2.857 mm) length and 0.135 in. (3.429 mm) width, the question is whether the maximum resistivity value will give a total resistance within the 1% required for final value.

$$\frac{.1125''}{.135''} = 0.8333 \text{ squares}; (0.8333) (120 \Omega / \square) = 99.999$$

Such a change in dimensions would be acceptable. If such a maximum resistivity did occur, no trimming would be required. When manual trimming equipment is being used, the elimination or reduction of any trimming operation is significant.

All the previous trimming was used to raise the resistor value. The following sketches illustrate how resistor designs can incorporate the capability for raising or lowering the resistor value in incremental steps.

7.8.2 (Cont.) Thin Film Resistor Design



Derivation of Equation for Determining the Minimum Trimming Length.

If the total resistance change (from lowest possible value to final value) is to be accomplished by trimming one bar, then an expression is needed which equates that total change to the difference in value of the trim bar before and after trimming. Then the difference in value of the trim bar can be expressed

7.8.2 (Cont.) Thin Film Resistor Design

as a function of its dimensions and its minimum resistivity. Since the minimum resistivity and the widths (before and after trimming) are known, the equation becomes an expression of the only remaining unknown, namely the required minimum length.

(Trim bar value after trimming) minus (Trim bar value before trimming) equals (Total value change of resistor)

$$\begin{aligned}\text{Trim bar value after trimming} &= (\text{Number of squares after trim}) \\ &\quad (\text{Min. Rstv.}) \\ &= \frac{\text{Trimming Length}}{\text{Width after trim}} (\text{Min. Rstv.})\end{aligned}$$

$$\begin{aligned}\text{Trim bar value before trimming} &= (\text{Number of squares before trim}) \\ &\quad (\text{Min. Rstv.}) \\ &= \frac{\text{Trimming Length}}{\text{Width before trim}} (\text{Min. Rstv.})\end{aligned}$$

$$\begin{aligned}\text{Total value change of resistor} &= (\text{Final Value}) - (\text{Min. possible value}) \\ &= (\text{Final Value}) - (1 - \text{Rstv. Tol.}) \\ &\quad (\text{Design Value})\end{aligned}$$

Substituting into the original expression gives:

$$\frac{(\text{Trimming Length})(\text{Min. Rstv})}{(\text{Width after trim})} - \frac{(\text{Trimming Length})(\text{Min. Rstv.})}{(\text{Width before trim})} = (\text{Final Value}) - (1 - \text{Rstv. Tol.}) (\text{Design Value})$$

Factoring the left side of the equation gives:

$$(\text{Trimming Length}) \left[\frac{(\text{Min. Rstv.})}{(\text{Width after trim})} - \frac{(\text{Min. Rstv.})}{(\text{Width before trim})} \right]$$

7.8.2 (Cont.) Thin Film Resistor Design

Dividing both sides of the equation by the expression in square brackets gives:

$$\text{Trimming length} = \frac{(\text{Final Value}) - (1 - \text{Rstv. Tol.}) (\text{Design Value})}{\frac{(\text{Min. Rstv.})}{(\text{Width after trim})} - \frac{(\text{Min. Rstv.})}{(\text{Width before trim})}}$$

The above equation expresses the minimum trimming length that must be available to provide for the maximum possible trimming requirement. If the actual resistivity turns out to be greater than its possible minimum, the required value change will be less. Then the trim bar need not be trimmed for its full length or to its minimum width.

7.9 THICK FILM MULTILAYER SUBSTRATES

There are two common configurations of thick film multilayer substrates; the dimensional constraints within those two basic types vary to suit the materials, equipment, and techniques being employed.

The two basic configurations are "dielectric cross-over bridges" and "continuous dielectric multilayer."

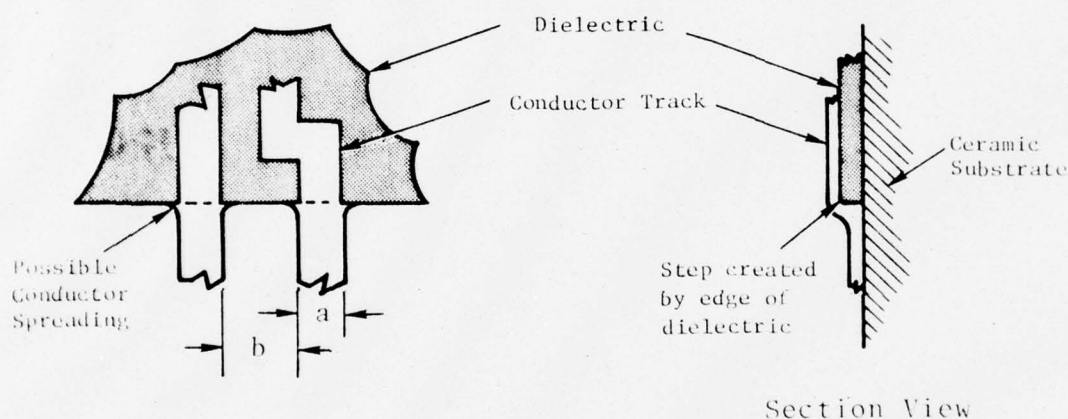
"Cross-overs bridges" are isolated patches of dielectric material. The conductor tracks printed on top of these bridges make contact with first-level tracks by overflowing the edges of the dielectric patches. This cross-over configuration is usually limited to two levels of conductors. The "continuous dielectric" is a complete layer of dielectric material, and the interlevel connections are made through holes (called "vias") in the dielectric layers. The number of levels available has no inherent limit; it is limited only by the processing variables.

The following sections (7.9.1 and 7.9.2) will not define specific dimensional limits. They will depict various details of the two types of thick film multilayers and will call attention to those dimensions that need to be specified by the manufacturing group that will fabricate the substrates.

Reminder: Each application of additional paste material (either conductive, resistive, or dielectric) is accomplished with subsequent screen masks. Alignment targets should be provided on each artwork for accurate registration.

7.9.1 Multilayer Substrates Using Dielectric Cross-Over Bridges

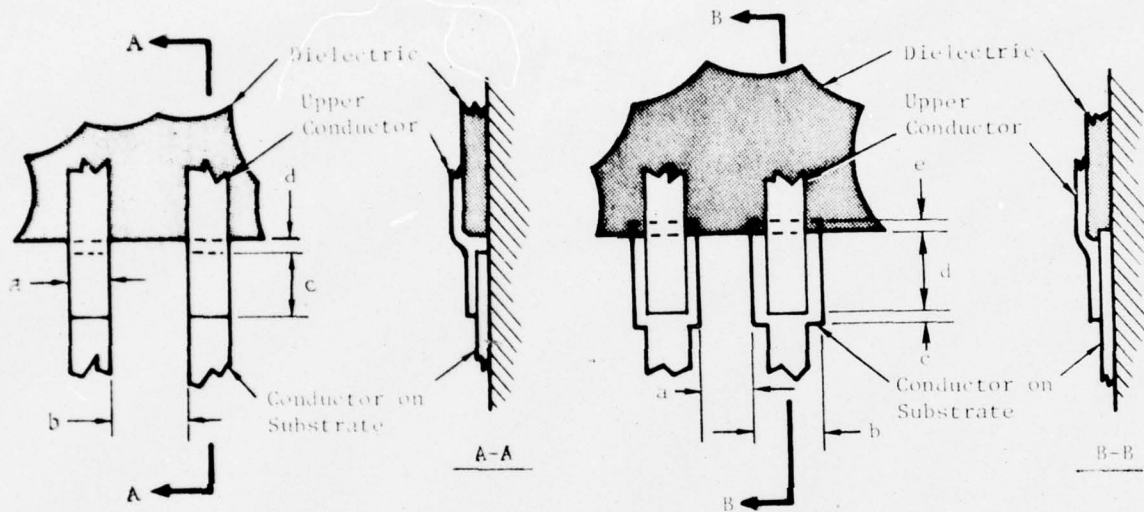
Where a conductor track crosses the edge of the dielectric bridge, there is a possibility that the conductor paste will spread along the dielectric edge. This happens because the step created by the dielectric edge causes a gap under the screen which permits excess conductor paste to flow through, and under, the screen.



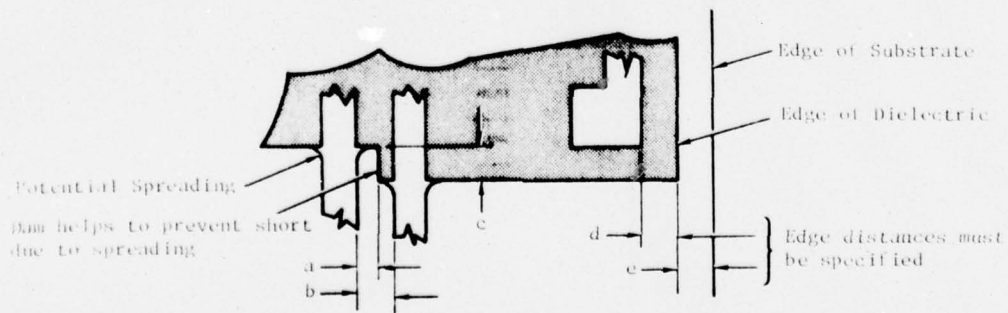
The possibility that a conductor track may spread usually necessitates allowing for additional space between tracks at the dielectric edge.

The conductors above the dielectric make contact with the conductor tracks on the substrate surface by overflowing the dielectric edge and overlapping onto the lower tracks. The plan view and cross-section of two configurations are illustrated in the following sketches. Dimensions a, b, c, d, e are the overlap dimensions and the relation to the dielectric edge. These dimensions need to be specified by the manufacturing group.

7.9.1 (Cont.) Multilayer Substrates Using Dielectric Cross-Over Bridges

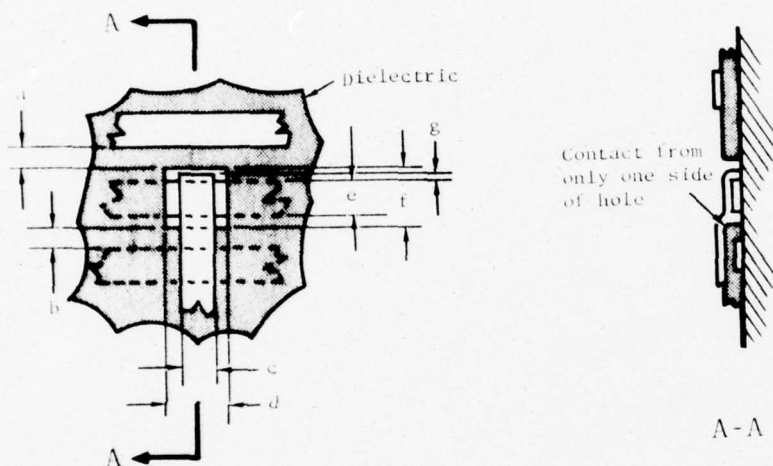


The dielectric can be shaped to form a dam that can help prevent an electrical short due to spreading of adjacent conductors.

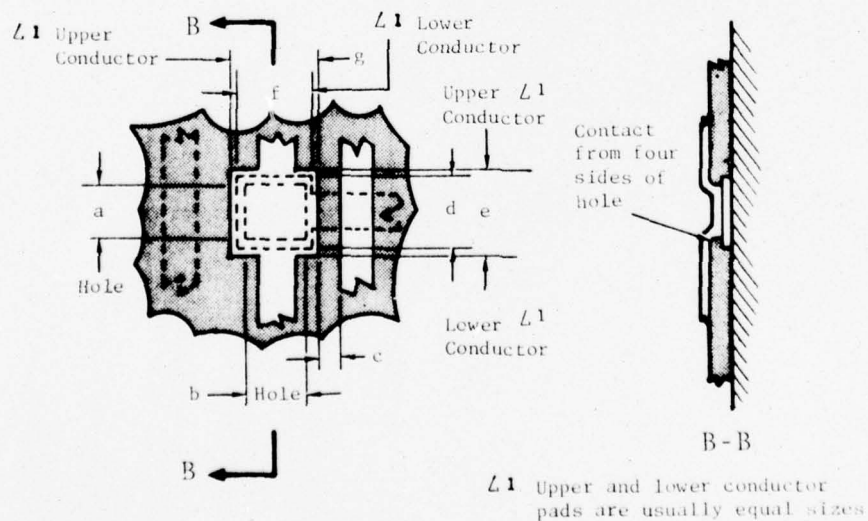


7.9.1 (Cont.) Multilayer Substrates Using Dielectric Cross-Over Bridges

Contact between conductors can also be made through a hole in the dielectric. The upper conductor is intended to flow down into the hole to overlap the lower conductor. This is not the same as using a "via-fill." (See Section 7.9.2.) One configuration is shown below.



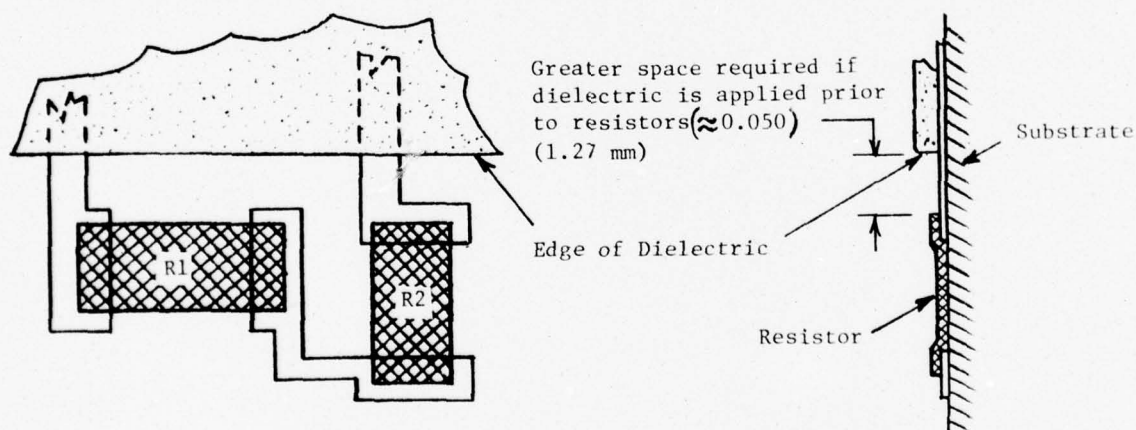
Another common configuration has pads larger than the hole in the dielectric.



7.9.1 (Cont.) Multilayer Substrates Using Dielectric Cross-Over Bridges

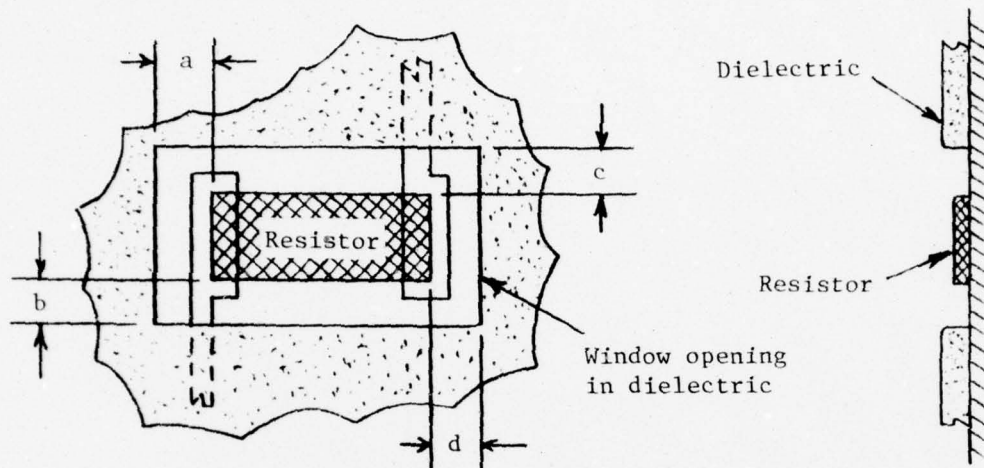
Resistors can be fabricated on a multilayer substrate. They are usually fabricated on the surface of the substrate, in an area devoid of multiple layers.

It is desirable to fabricate the resistors after the multiple layers in order to avoid changes to the resistor values caused by subsequent firing cycles. However, when the resistors are fabricated after the multiple layers, the resistor screen/squeegee must pass over the step created by the dielectric edge. Screening the resistor paste on such a stepped surface requires greater space between the resistor and any nearby step.



Resistors "down-in-a-hole" can only be screened prior to the dielectric. Clearance dimensions should be specified by the manufacturing group, and the resistor design must compensate for the changes in resistivity due to subsequent firing. The compensation must be specified by the manufacturing group, who can only make such a determination after experimenting with the particular paste.

7.9.1 (Cont.) Multilayer Substrates Using Dielectric Cross-Over Bridges



7.9.2 Multilayer Substrates Using Continuous Dielectric Layers

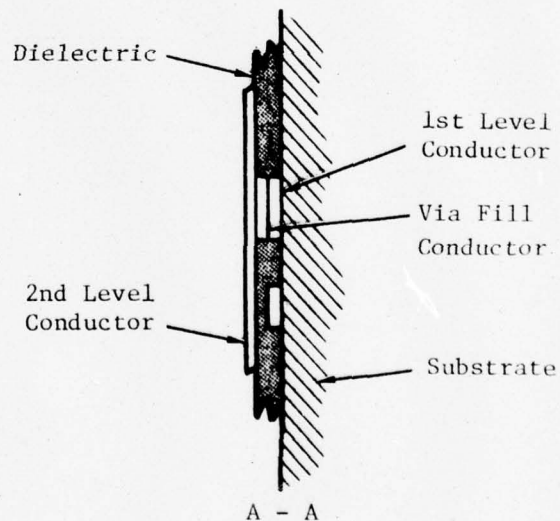
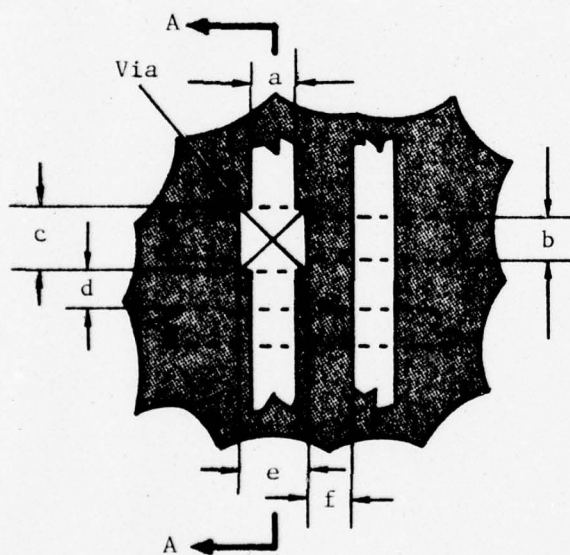
A continuous dielectric layer is an uninterrupted plane of dielectric material. The first layer to be applied on the bare ceramic is always a conductor (metallization) layer, the configuration can be either a pattern of tracks or a continuous plane. The continuous dielectric layer is applied over the conductor layer. Another conductor layer goes on top of the dielectric. This alternating sequence can be repeated to create several layers of conductor tracks, each one separated by a dielectric layer. Conductors on separate layers are interconnected through small holes in the dielectric layer. These holes are called "vias."

The overflow-conductor technique (as shown in Section 7.9.1) can be used with continuous dielectric layers, but the size of the vias must be large, and two vias cannot be in direct vertical alignment. The most common technique is to apply a "via-fill"

7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers

metallization step to the processing sequence. The via-fill step is a separate application of conductive metallization that fills only the vias, thus bringing the level up flush with the dielectric plane. Using a separate via-fill metallization improves flatness and thereby increases the number of layers possible. This method does, however, increase the number of screen-and-fire processing steps.

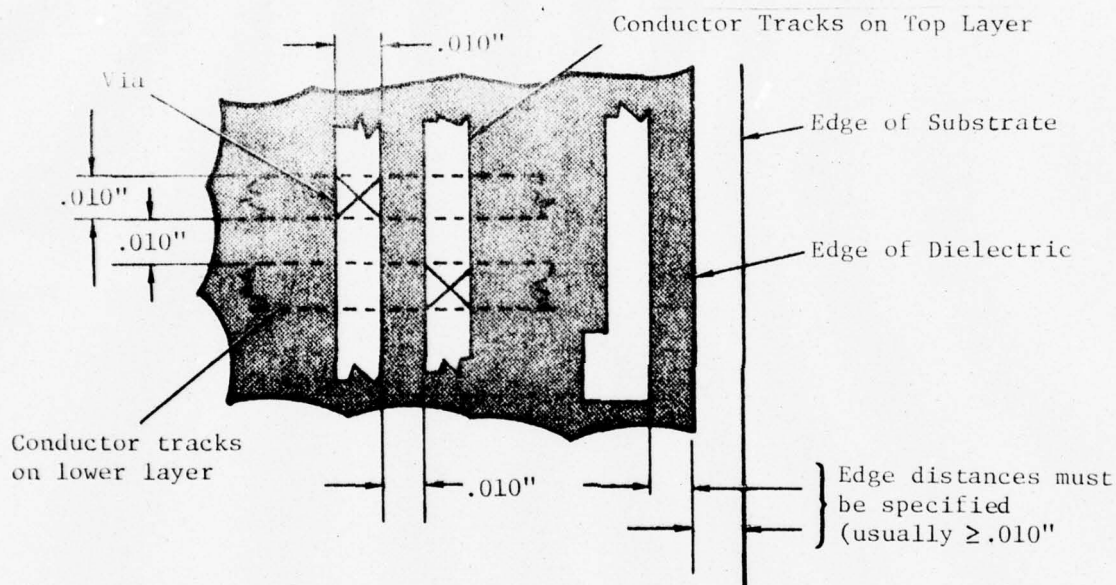
For continuous-dielectric configurations, the dimensions of the vias and mating conductor tracks must be specified to suit the manufacturing requirements.



Filled-via techniques have produced substrates having six conductor layers with 5 mil (0.127 mm) lines and 7.5 mil (0.1905 mm) spaces. However, such densities are not recommended for high-volume production.

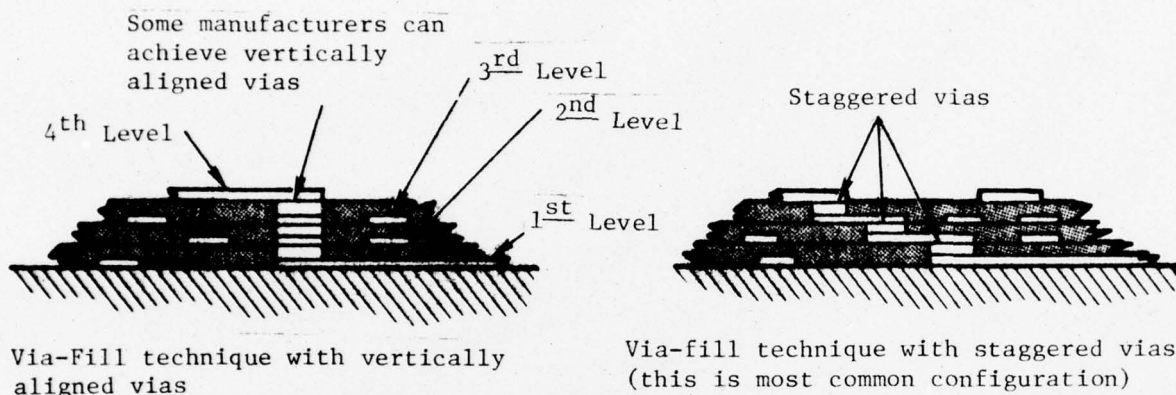
7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers

Filled-vias have been made, with consistently good yields, at a size of 10 mils (0.254 mm) by 10 mils. The mating conductors were 10 mil lines and 10 mil spaces. Such a configuration would appear on a layout as follows:



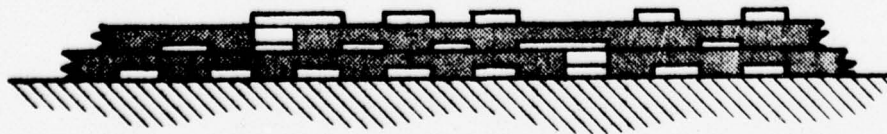
The relationship between subsequent vias varies with different manufacturers. The most common groundrule is that subsequent vias cannot be in direct vertical alignment. However, some manufacturers have achieved acceptable yields with vertically aligned vias. Vertical alignment requires less area than staggered vias, thereby permitting higher density.

7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers



In all multilayer fabrication, as each layer is applied, maintaining the flatness of the top surface becomes increasingly difficult. Lack of flatness sometimes necessitates increased dimensions for both line widths and spaces. The manufacturing group should specify the dimensions required for all layers.

It is good practice to stagger the positions of conductor lines with respect to the vertical alignment with other lines on adjacent layers. This staggering tends to improve the flatness of each successive layer, reduces electrical cross-coupling, and reduces the chances for interlayer shorts through pin holes in the dielectric.



7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers

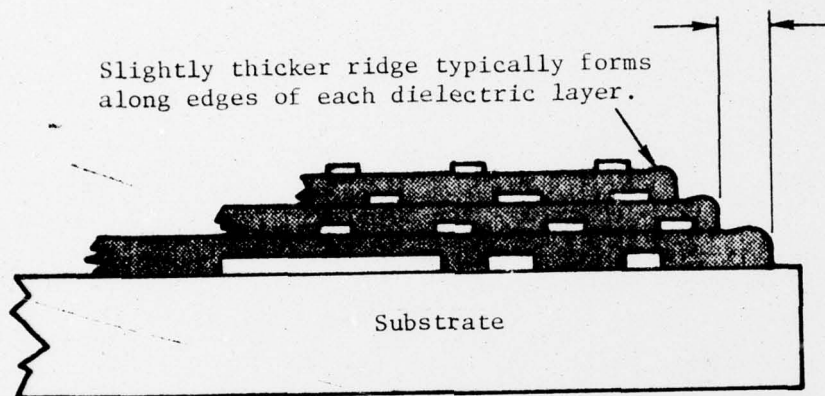
Integral resistors can be applied directly on top of multiple layers. Resistor paste is available (from certain material manufacturers) whose composition is compatible with dielectric material used for multilayer fabrication.

If a resistor is to be on top of multiple layers, and the resistor is to be laser trimmed, there should be no conductors directly below the area of trimming. There is a high probability that the laser energy will burn through to lower layers. Abrasive trimming is worth consideration in these circumstances.

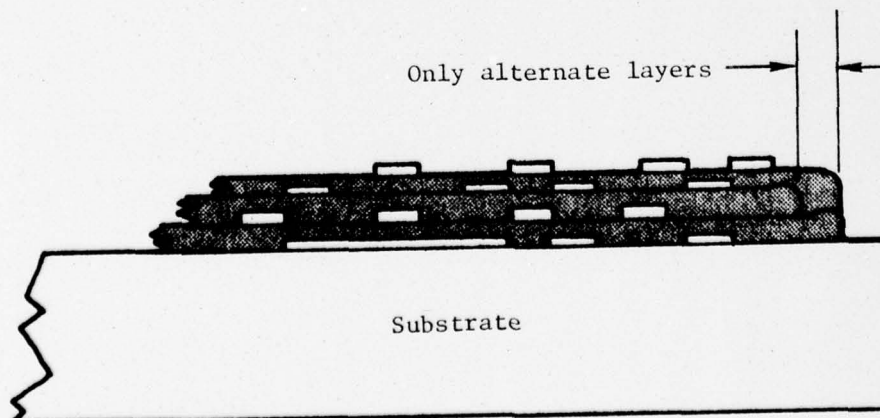
It is not recommended that multiple layers be applied directly over resistors because changes to the resistors will occur. The changes are caused primarily by the temperature of subsequent firings. Changes can also occur due to variations from one lot of paste to the next lot. Only by experimenting with an individual lot can a prediction be made of subsequent changes. So, while multiple layers can be applied over resistors, this practice cannot be recommended for production quantities.

It is often necessary (depending upon the processing requirements) that the outside edges of each subsequent dielectric layer be inset from the edge of the previous layer. The reason for the setback of subsequent layers is that a slightly thicker "ridge" typically is formed around the outer edge of the dielectric layer. The manufacturing group should specify the dimensions.

7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers

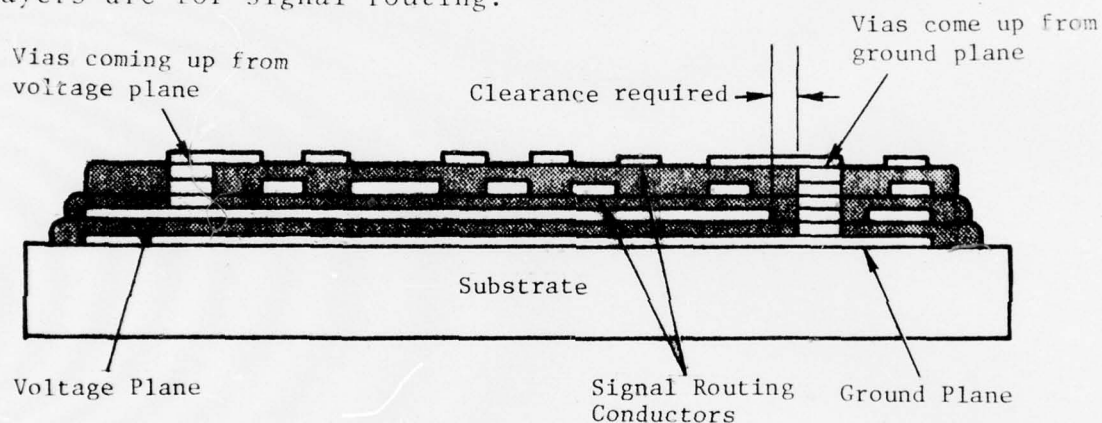


Another configuration that has been used to offset the extra thickness of the outer edges is to set back only the alternate layers. This retains more usable area than set back of every subsequent layer.



7.9.2 (Cont.) Multilayer Substrates Using Continuous Dielectric Layers

One particular multilayer configuration is noteworthy. The first two conductor layers are continuous planes. They will be the electrical voltage and ground planes. The dielectric between the two can be of a high-dielectric material, thus creating a filter capacitance between the two planes. The subsequent conductor layers are for signal routing.



Note: Vias may be either vertically aligned (as shown) or in a staggered arrangement.

One major expenditure encountered in fabricating multilayer substrates is the time required to test the substrate for internal shorts or open circuits. During the layout, every effort should be made to facilitate the substrate checkout.

7.10 LAYOUT DESIGN REVIEW

It has proven to be very useful, when reviewing a hybrid design, to record and later file the design data. Besides providing answers to many of the questions that will arise later, a tabulating of the design data can act as a check-off list during the final design review.

If, during the design review, the data are recorded on a pre-printed form, the act of filling out such a form constitutes a checkoff of pertinent design criteria.

When the designer knows while he is creating the design that he will be responsible for providing answers to questions about temperature rise, maximum current and wattage, line and space density, potential problems in fabrication or testing, then such knowledge usually acts as a yardstick by which he measures each decision he makes during the design. The result is that better designs emerge, requiring very little redesign.

The following form called "Hybrid Circuit Design Summary Data" is presented as one example of a preprinted data sheet.

7.10 (Cont.) LAYOUT DESIGN REVIEW

HYBRID CIRCUIT DESIGN SUMMARY DATA	
Hybrid Name <u>LOGIC AND FET MULTIPLEXER</u>	Responsible Hybrid Engineer _____
Part Number _____	Draftsman _____
Date <u>11 MAY '76</u>	Responsible Circuit Designer _____
Hybrid Function <u>MULTIPLEXES THE CURRENT THROUGH THE DRIVER BANDS</u>	
<p>1. Package Size <u>1.50" X 0.600"</u> Estimated Weight _____</p> <p>2. Total Power Dissipation <u>2.25 W</u> Package: <input type="checkbox"/> BeO <input checked="" type="checkbox"/> Kovar</p> <p>3. Type of Substrate: <input type="checkbox"/> Thin Film, <input checked="" type="checkbox"/> Multilayer Thick Film. Number of Layers <u>4</u>, Number of Resistors Integral to Substrate <u>NONE</u>. <input type="checkbox"/> Voltage Plane, <input checked="" type="checkbox"/> Ground Plane.</p> <p>4. Typical line-to-line spacing <u>0.010</u>, Typical line width <u>0.010</u>, Closest line-to-line spacing <u>0.010</u>, Smallest line width <u>0.010</u>, Type Wire <u>AL ALY</u>, Wire size <u>0.001</u>.</p> <p>5. Power Requirements: Voltages <u>+5V +15V -15V</u>, maximum current in any line or lead <u>0.5A thru Q1</u>.</p> <p>6. Number of package leads available <u>26</u>. Quantity used <u>22</u>.</p> <p>7. Number of Test Points brought out of package <u>6</u>.</p> <p>8. Number of Components: <u>25</u> Total. (a) Resistors <u>9</u> (b) Capacitors <u>5</u> (c) Transistors and Diodes <u>6</u> (d) Integrated Circuits <u>5</u> (e) Magnetics <u>NONE</u> (f) Others (includes select-at-test items) <u>NONE</u>.</p> <p>9. Explain any anticipated fabrication problems <u>NONE</u></p> <p>10. Explain any anticipated test problems <u>NONE</u></p> <p>11. For hybrids dissipating more than three (3) watts, identify the hottest chip (greater than one second steady state condition) <u>N/A</u> Estimate the hot spot temperature of the hottest chip above the hybrid mounting surface temperature: AT <u>150°C</u></p>	

8.0 ARTWORK CRITERIA

The microcircuit artworks, generated in conformance to the design layout, are the patterns of the conductive, resistive, and dielectric materials used to fabricate the substrate. For each substrate design, there will usually be as many artworks as there are different materials or different material applications in the fabrication processes.

The enlarged artwork should always be created on stable material. Sheet mylar having a minimum thickness of 0.005 (0.127 mm) is almost universally accepted. The mylar film can be either clear or frosted.

The artwork should be generated at the same scale as the design layout. This permits the layout to be used as an underlay while the artwork is being created. The most commonly used scale for hybrids is 20x. Many photo vendors can make a 20x reduction in one camera shot.

Artwork patterns have been generated by methods ranging from black ink on frosted mylar, to computer controlled photoplotting at 1x scale. There are, however, two common methods of generating hybrid artworks. One is to manually apply tape onto sheet mylar. The other is to cut and peel pre-laminated polyester masking film. (The masking film is commonly called "Rubylith", although Rubylith is actually the trade name of one particular brand.) The cutting can be performed manually or by the use of a precision coordinatograph, the accuracy of which is $\approx \pm 0.001$." The choice of one of the two methods is dependent on the accuracy required. (If the artwork is created at 20x scale, any inaccuracies are reduced by a factor of 20 at the 1x scale.) If each layout line is on an exact grid position, tape can be manually placed to match the precision grid lines. The layout itself can be drawn directly on

8.0 (Cont.) ARTWORK CRITERIA

such a precision grid or one can be placed under the layout while the artwork is being created.

For manual taping, red vinyl tape is recommended which can be purchased precut to widths having a tolerance of $\pm 0.003"$ (0.0762 mm). Presuming 20x scale for the original artwork, 0.003" variation becomes 0.00015" (0.00381 mm) variation at 1x scale. This same red vinyl tape can be used to make changes or corrections to artwork created on cut and peel masking film. The coordinatograph cutting tip can also cut through the vinyl tape producing a sharply defined edge.

The black crepe tape often used for printed circuit artwork is not recommended. Compared to the vinyl tape, the edge of the crepe tape is more ragged; and more importantly, the crepe tape is subject to movement on the surface of the mylar. This movement may occur if the crepe tape is inadvertently stretched while being applied to the mylar. The adhesion to the mylar surface is under constant stress due to the tendency of the crepe tape to spring-back after having been stretched.

In every case, where more than one artwork is required for one substrate, there is an alignment relationship between the various artworks. Wherever possible, each artwork should contain alignment targets which correspond to targets on the other artworks. Such marks facilitate the proper alignment of the patterns to each other. It is convenient to have the alignment marks within the substrate area, since the marks will then appear on the physical part, and can be used as visual inspection points to check the alignment. However when space does not allow the marks to be within the substrate area, they should be placed in the border area of the films.

8.0 (Cont.) ARTWORK CRITERIA

In thin film processing, the 1x working film or glass is used repeatedly to expose the image on the substrate. Such repeated use increases the chances for the working image to become scratched, or damaged in other ways. It is too expensive to recreate working films by making a 20x reduction for each one. A 1x scale glass master is often generated from the original 20x artwork. The working films are generated by making contacts prints from the glass master.

The term "field" refers to the background of the image. Either the field or the actual pattern is opaque while the other is clear. The terms "clear field" or "dark field" are commonly used to describe the artwork or film. The "reading" of the film refers to whether the image is right reading through the film material, (i.e., the base); or whether the image is right reading when viewing the emulsion side of the film. The expressions "right-reading base" and "right-reading emulsion" are commonly used.

The glass master must be of the opposite field and opposite reading from the working film if the working film has a negative emulsion. If positive-emulsion film is used the glass master must have the same field but will still be opposite reading from the working film.

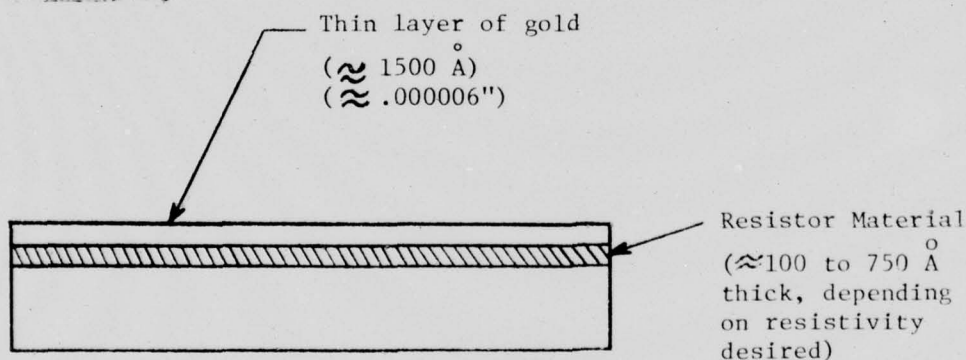
In Sections 8.1 and 8.2, particular requirements for thin and thick film artworks are delineated, with emphasis on the most important function of the artwork (i.e., its use in fabrication). The use in fabrication dictates the various requirements.

8.1 THIN FILM ARTWORK

The artworks described in this section are divided into two categories: artwork for pattern plating fabrication, and artwork for panel plating fabrication.

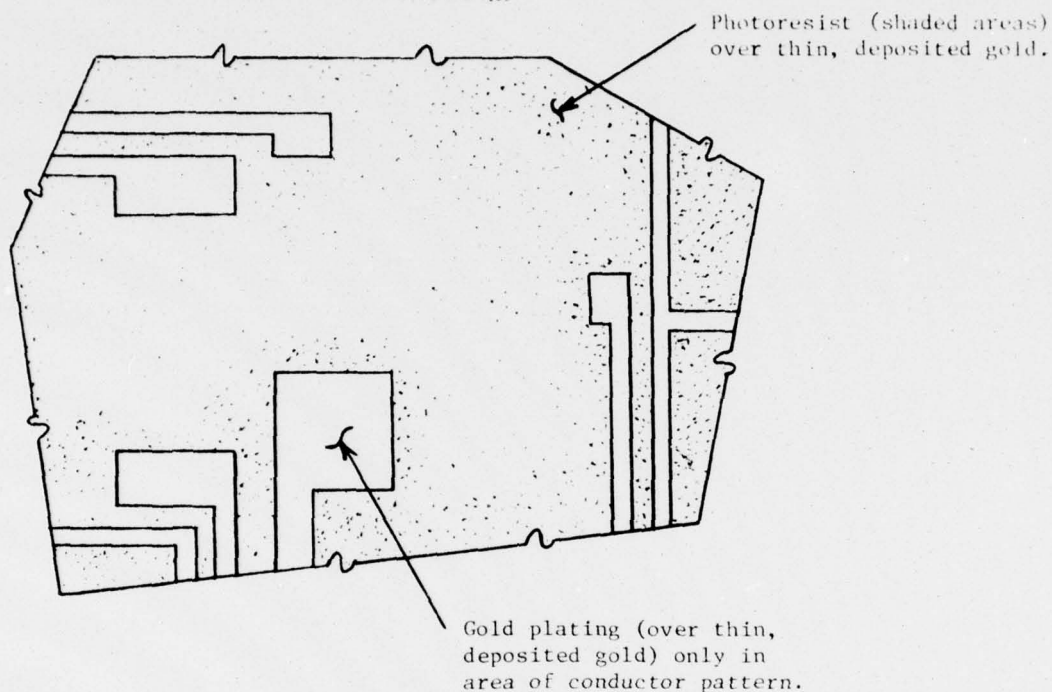
ARTWORK FOR PATTERN-PLATING FABRICATION

In the pattern-plating fabrication technique, a continuous layer of resistor material is deposited to the full thickness required (≈ 100 to 750 \AA , depending on resistivity desired). Next, a layer of gold is deposited on top of the resistor material just thick enough to make the top surface electrically conductive ($\approx 1500 \text{ \AA}$).



Photoresist is next applied over the entire surface. The conductor pattern is exposed and developed in the photoresist. The developing process exposes the thin gold in the conductor areas only. Within the exposed areas, gold is plated to the desired thickness, .1 mil (.00254 mm). The 1x-scale film or glass used to create the conductor pattern must be right-reading base (i.e., right reading with the emulsion on the far side) because the emulsion must make contact with the photoresist. (In some mask-alignment equipment no contact is made, but the emulsion on the mask should still be close to the photoresist.) The image can be a clear or dark field depending on whether the photoresist is negative or positive.

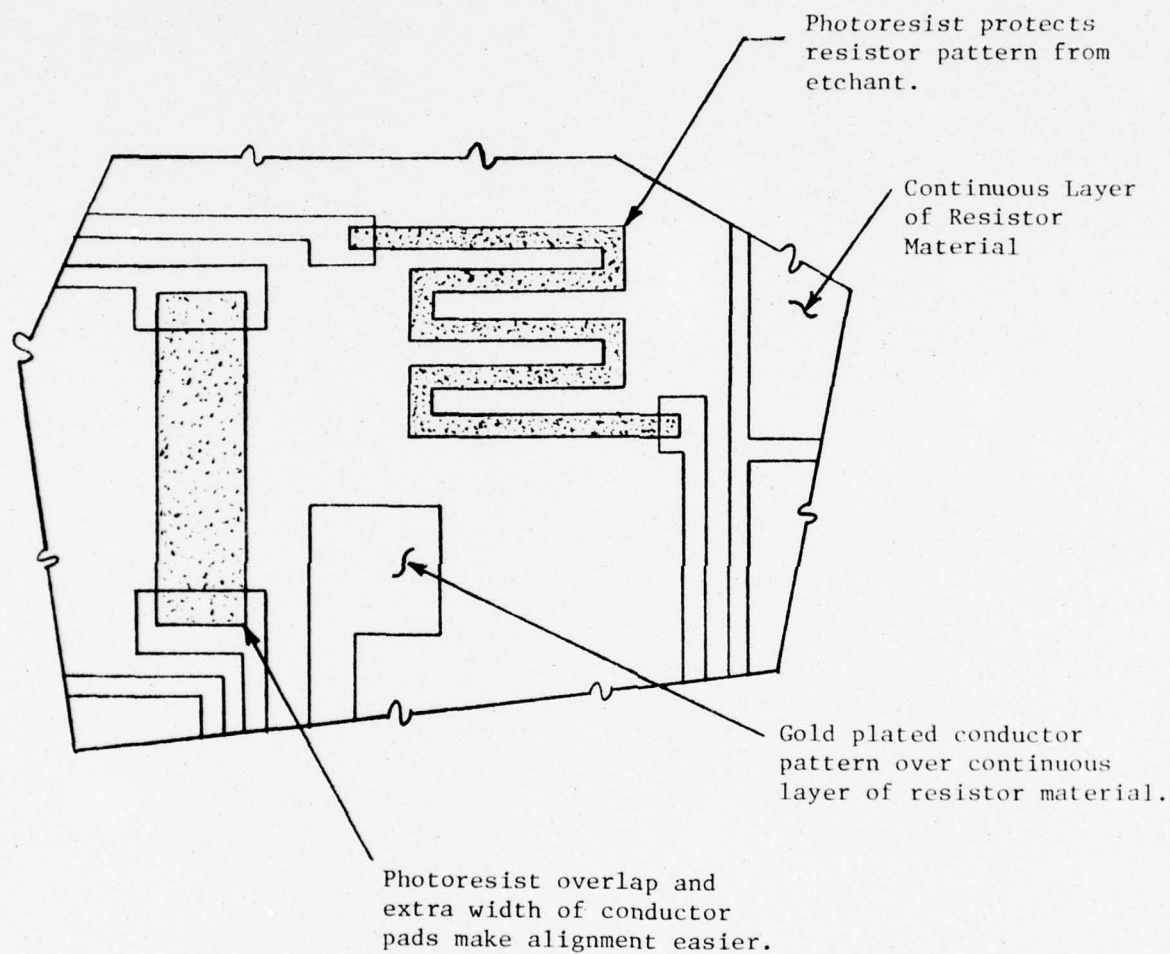
8.1 (Cont.) THIN FILM ARTWORK



After plating, the photoresist is removed. The gold is then etched in acid until all of the thin gold is removed. (The surface of the plated gold is also etched; but since the plated gold is approximately 16 times thicker than the deposited gold, the amount of etch on the plated gold is insignificant.) The surface now consists of the gold conductor pattern over a continuous layer of resistor material.

Next a new layer of photoresist is applied. The resistor pattern is then exposed and developed. This developing process removes photoresist everywhere except the actual resistor pattern. The working-film can be either clear or dark field, depending on whether the photoresist is negative or positive, but it must be right reading-base to contact the emulsion to the photoresist.

8.1 (Cont.) THIN FILM ARTWORK

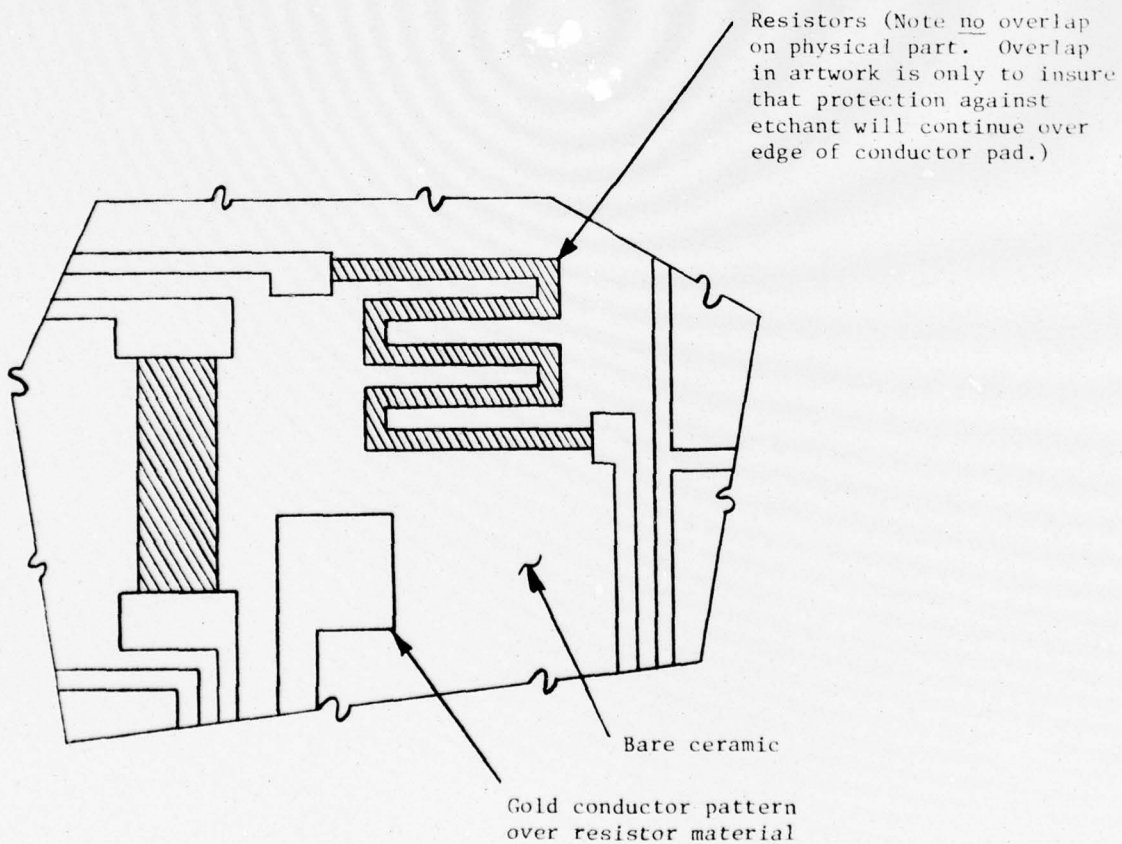


The layer of resistor material is next etched away, except where the gold and photoresist prevent etchant contact. The last step is to remove the remaining photoresist, thus exposing the resistor patterns.

8.1 (Cont.) THIN FILM ARTWORK

Note that for pattern-plating the resistor pattern overlaps the conductor and the conductor is wider than the resistor.

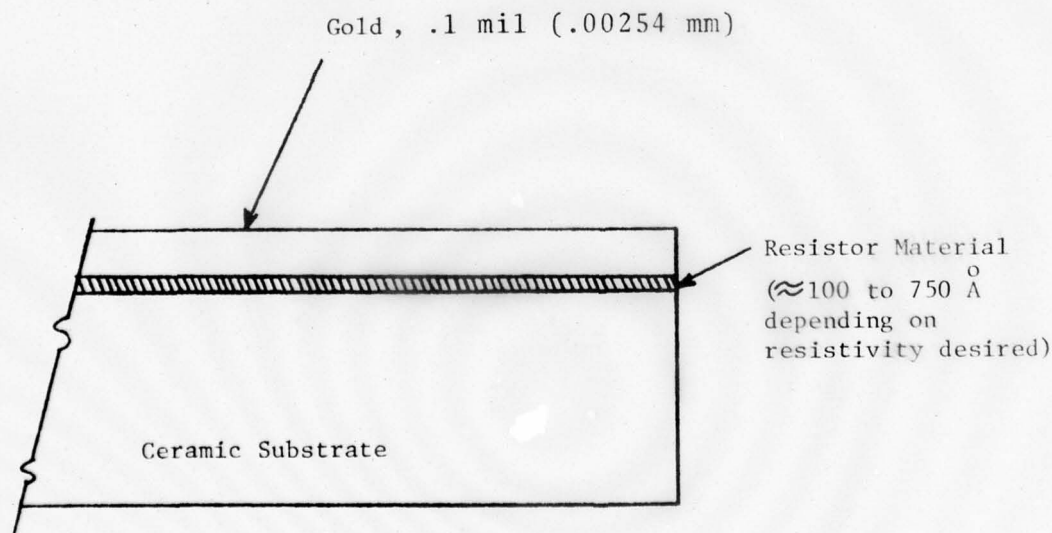
The finished substrate looks thus:



8.1 (Cont.) THIN FILM ARTWORK

ARTWORK FOR PANEL PLATING FABRICATION

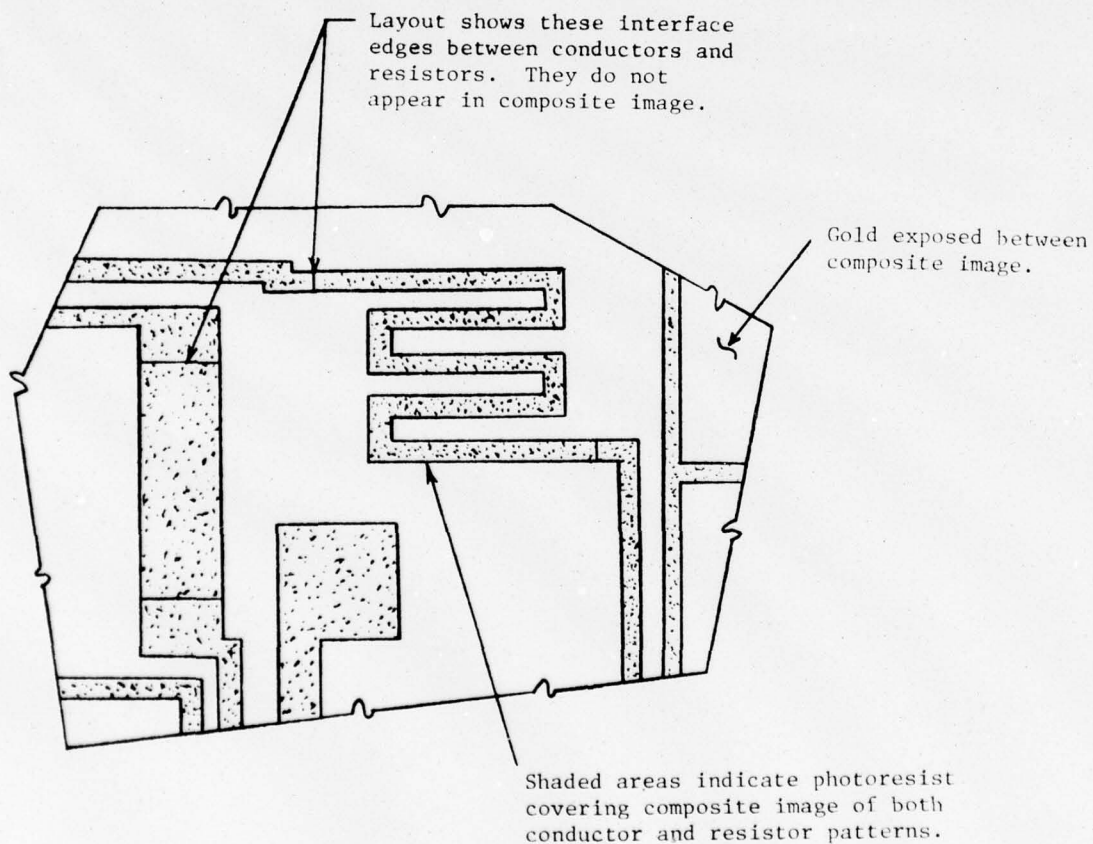
In the panel-plating fabrication technique, a continuous layer of resistor material is deposited on the bare ceramic substrate to the required final thickness (≈ 100 to 750 \AA , depending on the resistivity desired). Next, a continuous layer of gold is applied over the resistor material to the required final thickness ($\approx 100 \text{ \mu in.}$). The gold layer is usually applied by vacuum deposition sufficiently thick to make the surface conductive, then plated to achieve the desired final thickness.



Photoresist is next applied over the entire surface. A composite image of both the conductor and resistor patterns is then exposed and developed in the photoresist such that the gold is exposed only in the areas between the composite image (hardened photoresist covers only the composite image). The working film (or glass) used

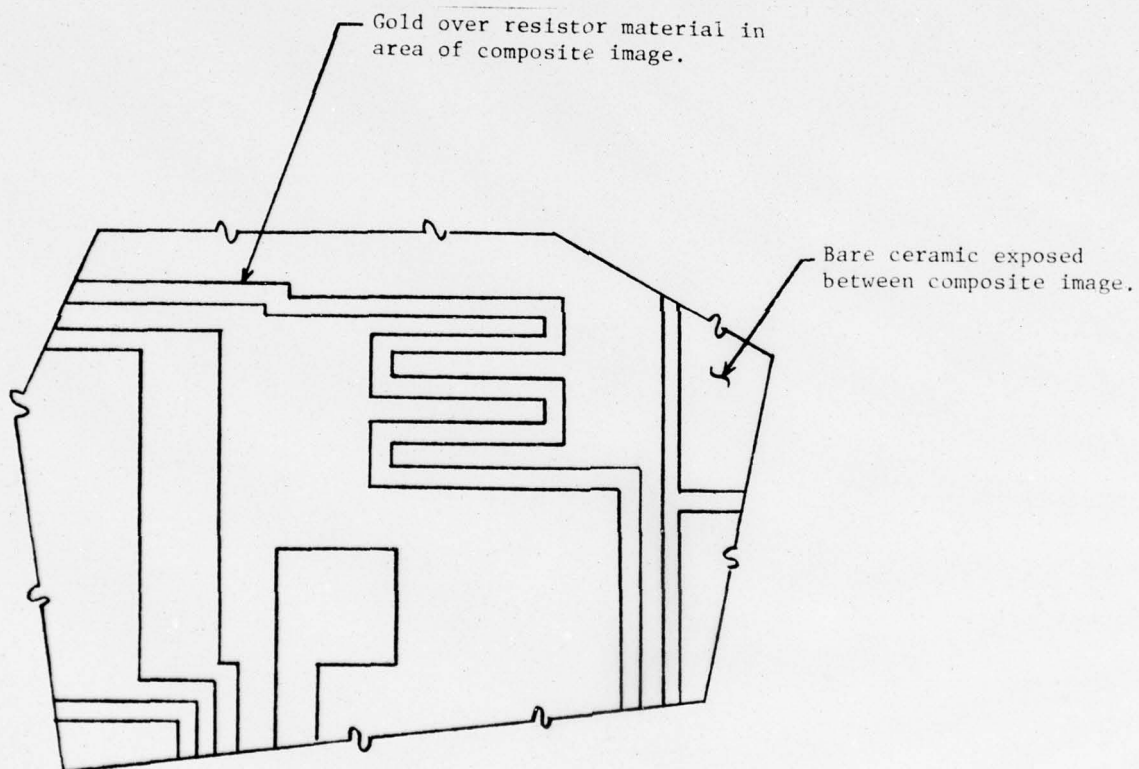
8.1 (Cont.) THIN FILM ARTWORK

to create this image must be right-reading-base so that the film emulsion makes contact with the photoresist. (If certain mask-alignment equipment is used no contact is made, nevertheless the mask should be right-reading-base.) The working-film may be either light or dark field, depending on whether the photoresist is negative or positive.



8.1 (Cont.) THIN FILM ARTWORK

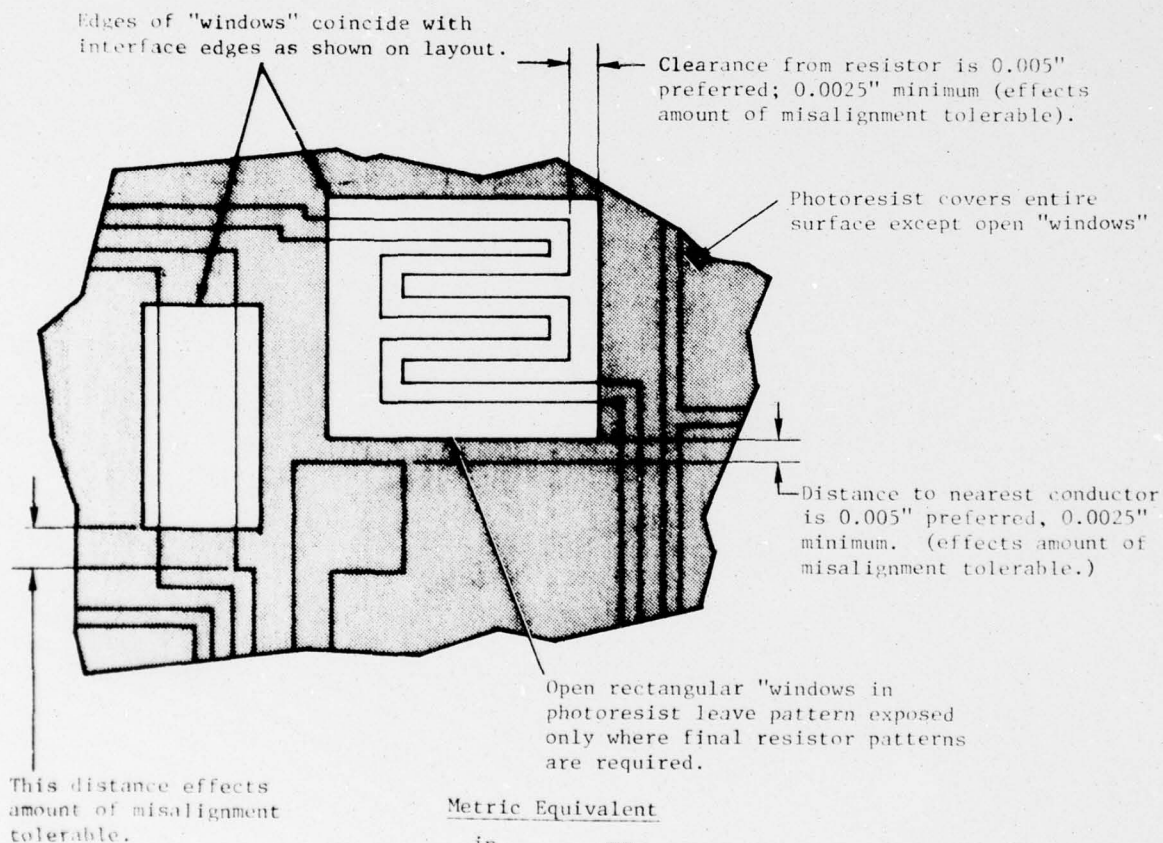
Next, both the gold and resistor layers in the exposed areas are etched down to the bare ceramic. (This is accomplished with two different etchants.) The photoresist covering the composite image is then removed. Within the composite image the surface of the substrate now has the gold over resistor material, and bare ceramic is exposed between.



A new layer of photoresist is then applied over the entire surface. An image is exposed and developed in the photoresist which leaves the resistor areas exposed within rectangular "windows."

8.1 (Cont.) THIN FILM ARTWORK

The working-film used to create these rectangular "windows" must be right-reading-base. It may be either light or dark field depending on whether the photoresist is negative or positive.



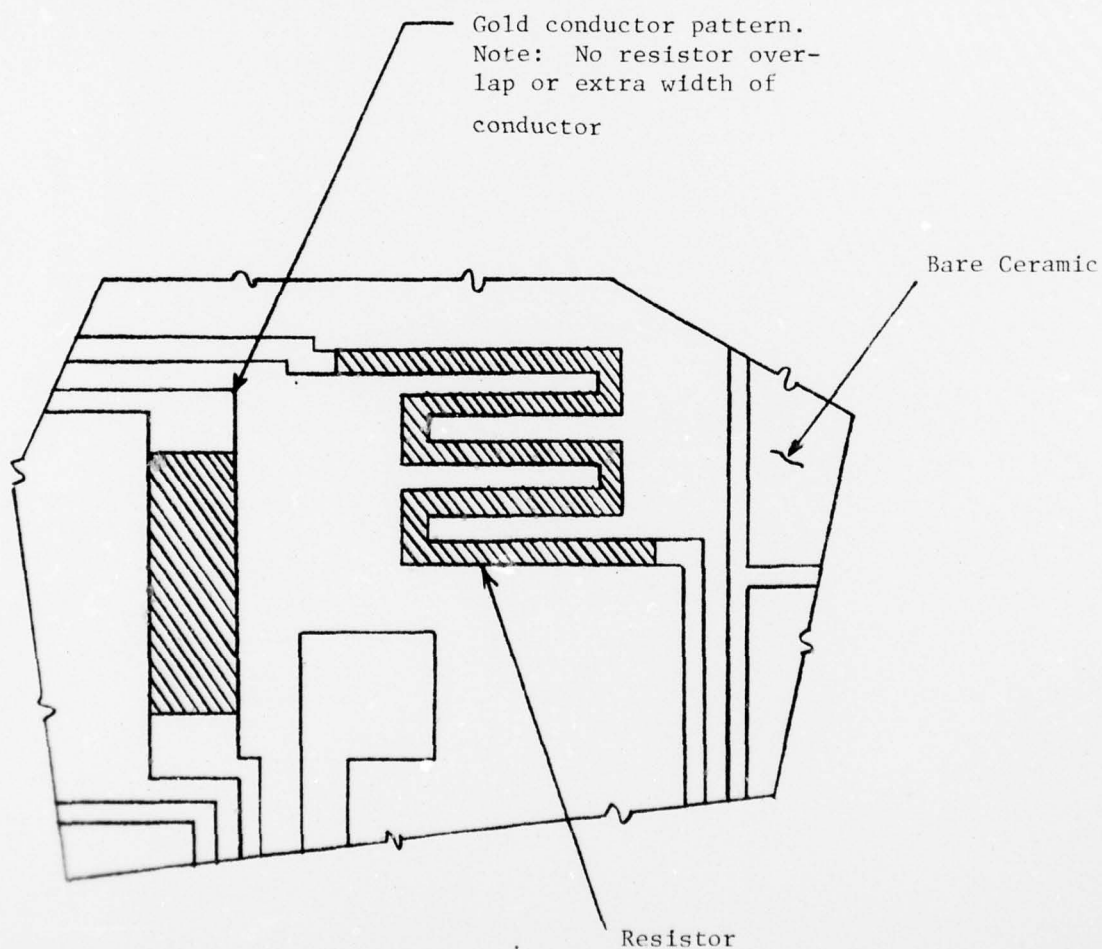
Metric Equivalent

in	mm
0.0025	0.0635
0.005	0.127

8.1 (Cont.) THIN FILM ARTWORK

Next a single etch is performed that removes only the gold within the window openings and leaves the resistor material. When the photoresist is removed, the substrate is complete except for any trimming that might be required for the resistors.

The final configurations looks thus:



8.2 THICK FILM ARTWORK

In thick film technology, 1x-scale film is not used directly on the substrate. Instead, the film is used to create the desired pattern on a screen, which is then used to deposit the material on the substrate.

Since the photosensitive emulsion on the screen is almost always a negative type (the emulsion "hardens" wherever light strikes), the 1x film should have a clear field and be right reading from its emulsion side. Figure 8.2-1 shows the relationship of the film and the screen.

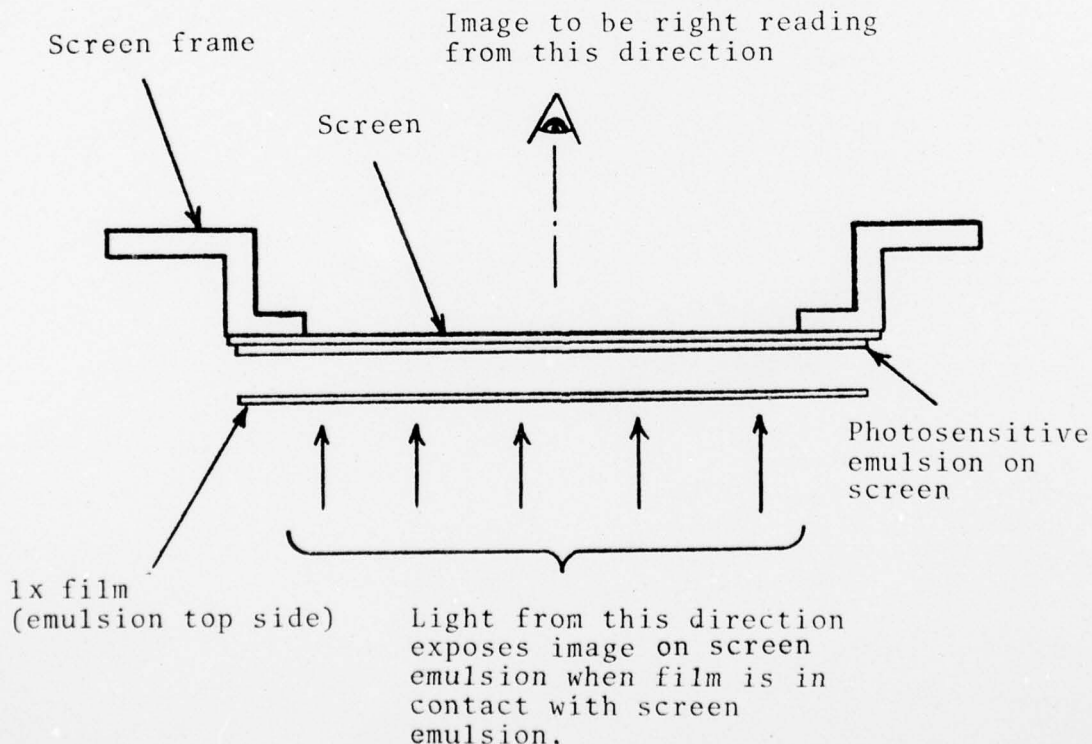


FIGURE 8.2-1 RELATIONSHIP OF FILM AND SCREEN

8.2 (Cont.) THICK FILM ARTWORK

It is also desirable to have alignment marks within each pattern. Such marks would appear in each application of the thick film paste on the substrate and would thereby provide for quick visual inspection to confirm the correct alignment of the patterns to each other. Whenever space permits, such internal alignment marks should be used. Whenever multiple layers are applied, the relationship of the vias in the dielectric layer and the via-fill metallization automatically provides such visual inspection points.

Since thick film patterns are applied by squeezing the paste through the patterns in the screens, there is usually a small increase in the width of a conductor line (comparing the size on the substrate to the size on the film). This increase depends on the viscosity of the paste and the pressure applied by the squeegee. While approximately one mil increase is typical, the actual increase to be anticipated should be determined by the manufacturing group. When 10 mil lines and 10 mil spaces are used, there is usually no need to compensate for this small increase when creating the original artwork. But where narrower lines and spaces are needed, the need to compensate in the artwork should always be discussed with the manufacturing group.

With the exception of the compensation that might be required for narrow lines, the artworks for thick film are created to match the layout. And, unlike thin film substrates, the overlaps between resistors and conductors do appear on the actual substrate.

8.2 (Cont.) THICK FILM ARTWORK

The easiest way to create the 1x mask from the original 20x artwork is to make a 20x reduction with one camera shot. When the 20x artwork is generated by the cut-and-peel method the field is typically dark because it is much easier to peel the image area than the much larger field area. The high resolution film typically used for the 1x mask can be processed to make the image either dark or light. When the 20x artwork is generated by applying tape to mylar, the field is light but again the 1x film can be processed to give either light or dark field.

Each pattern to be applied to the substrate requires a separate screen. Each screen within the set of screens for one substrate, should have its pattern located within the screen such that the pattern aligns to the others of the set. Without a predetermined location of the pattern within the screen, each screen, after being installed into the printer must be aligned individually. This alignment within the machine can be very time consuming.

One easily implemented method of obtaining alignment from one screen pattern to another is to set up a fixture that locates each screen frame to a set of alignment marks within the fixture and to them locate each 1x film pattern to these same alignment marks, using corresponding alignment marks in the film.

These corresponding alignment targets in the film should be outside the actual pattern (i.e., should be in the border area of the film). The location of these targets should be outside the area of the largest pattern that can be anticipated, in order that the one fixture can be used universally. Of course, the targets will appear in the screen since the total film image is created in the screen, but these can easily be blocked out.

8.3 STEP-AND-REPEAT CRITERIA

Whenever multiple images (usually arranged in rows and columns) of the same artwork are created on one film, the image is said to be "step and repeated."

Such a step-and-repeated image is most commonly used to fabricate many substrates simultaneously out of one larger piece of ceramic. (The larger piece is later broken into separate pieces.)

The step-and-repeat "cameras," used to create a multiple image pattern, are easily capable of maintaining tolerances of ± 0.5 mils (0.127 mm) between images. Some can hold ± 0.1 mil (0.0254 mm). Whenever ± 0.1 mil is required, the step-and-repeated image should be on glass, not on film.

Since the large ceramic will be broken into individual pieces, it follows that the center to center distance between images in the film is the same as the size of the individual pieces.

When space permits, crop marks that define the corners of the individual piece can be added to the artwork. These can be utilized to quickly inspect the step-and-repeated pattern to ensure that each image is properly spaced from its neighbor. These corner marks can also serve as a guide for the scribe line that will later be cut into the surface of the ceramic, prior to its being broken. Corresponding corner marks can also serve as alignment guides between resistor and conductor artworks.

Figures 8.3-1 through 8.3-3 show examples of corner crop marks.

8.3 (Cont.) STEP-AND-REPEAT CRITERIA

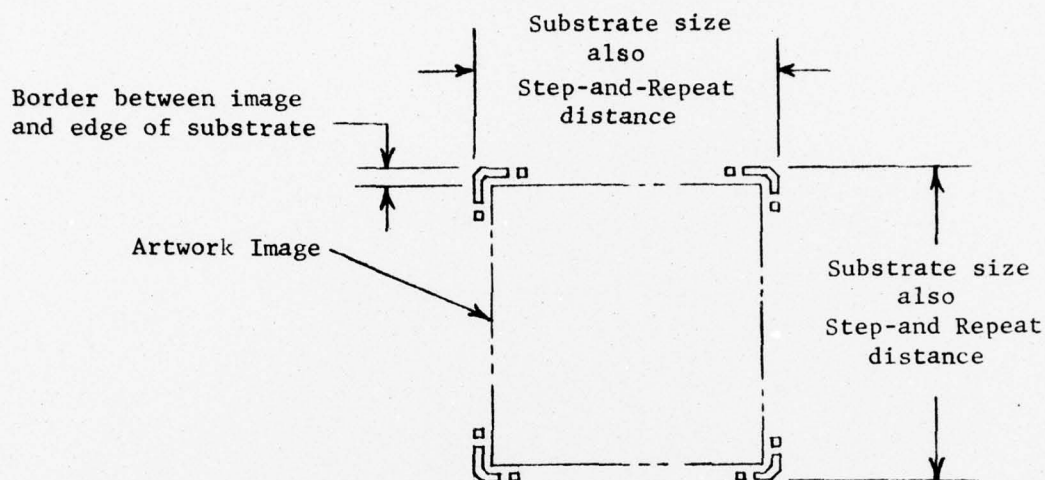


Figure 8.3-1 CROP MARKS IN INDIVIDUAL IMAGE

Alignment of adjacent notches indicates both horizontal and vertical alignment between adjacent images.

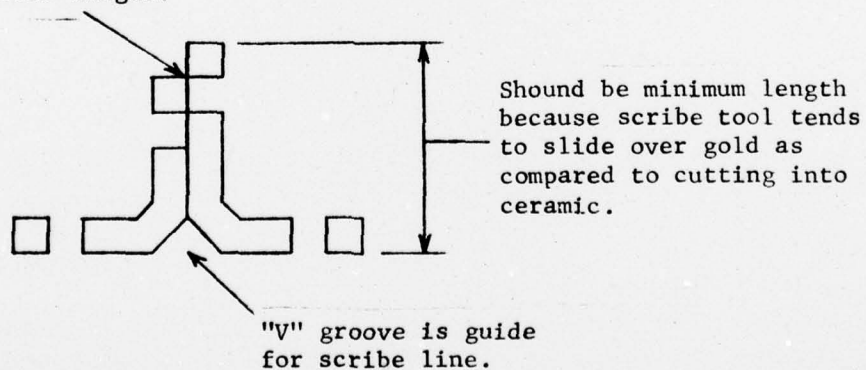


Figure 8.3-2 ENLARGED VIEW OF ADJACENT CROP MARKS

8.3 (Cont.) STEP-AND-REPEAT CRITERIA

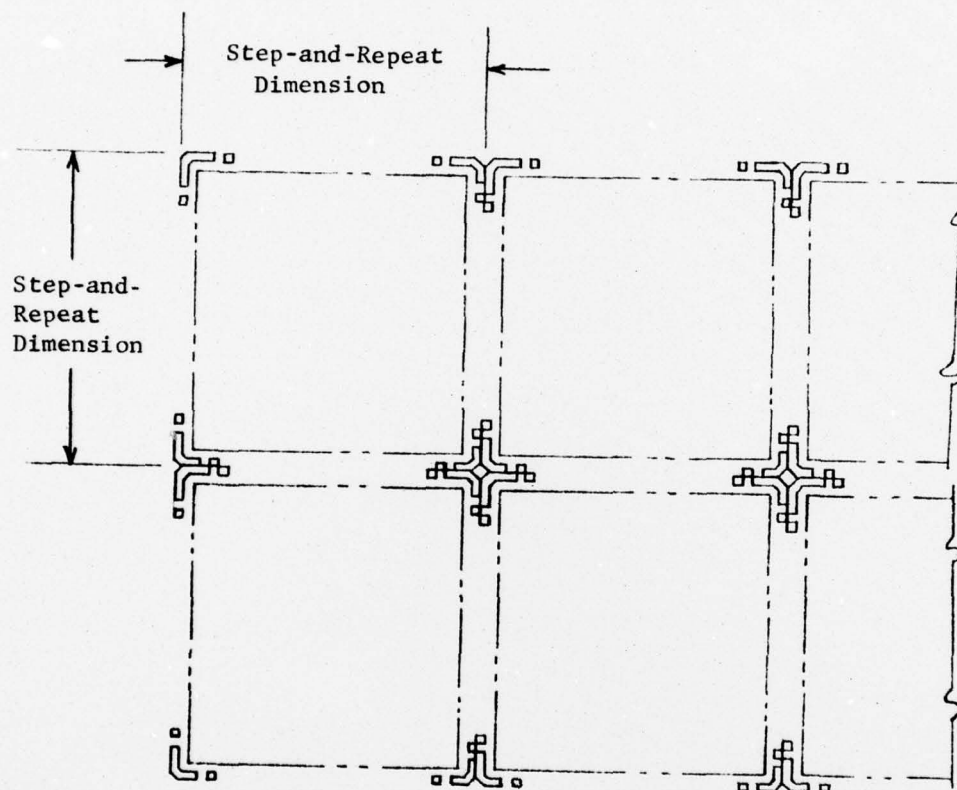


Figure 8.3-3 STEP-AND-REPEATED IMAGES

8.4 INSPECTION CRITERIA FOR 1x ARTWORK

The following is a listing of inspection criteria for 1x film or glass.

The degree of perfection required for each of the criteria depends on the content of the artwork (narrow or wide lines and spaces), the end use of the film, (thin film substrates or thick film screens), and the equipment that will be used with the film (collimated or non-collimated light). The fabrication group should be consulted for specific numerical criterion values or for graphic examples of acceptable photo quality.

The 1x film or glass should first be checked for accuracy of size. However, when several films are included in a set, the alignment of the members of the set to each other is sometimes more important than the actual size. A consistent small error can often be tolerated.

Pin holes in the opaque emulsion should be cause for concern. Of course, the maximum allowable size of any pin hole depends on where the pin hole occurs within the image.

Conversely, dark spots within the light areas of the image are undesirable. Again, the specific location determines the maximum allowable.

Scratches in the film have caused many defective substrates. This criterion should be checked periodically when the film is being used to fabricate thin film substrates.

The resolution (sharpness of edges) of the image is a criterion for which it is difficult to specify a numerical value. The

8.4 (Cont.) INSPECTION CRITERIA FOR 1x ARTWORK

edge between a light area and a dark area of an image may appear sharply defined at 10x magnification but might appear to be blurred or fuzzy at 50x magnification. The criterion is usually expressed as the amount of magnification required to detect a fuzzy edge.

The dark areas of any image should be truly opaque (not gray) when viewed with back lighting. The strength of the back lighting can be specified as the criterion to detect grayness.

SECTION 9 DOCUMENTATION REQUIREMENTS

The documentation for a hybrid microcircuit has the primary responsibility of defining the completed product, assigning an identification number to it, and recording the history of any changes to the configuration. Hybrids (unlike more established technologies) typically require more engineering control of the processes being used in manufacturing. This philosophy is intended to ensure high reliability and consistently high yields. The control is expressed in the engineering drawings. Therefore hybrid drawings exert a degree of control over manufacturing processes not usually seen on other engineering documentation. Even the manufacturing operations traveler is sometimes created by the engineering department.

Every engineering document should be assigned a number that is compatible with some standardized method of number assignment. Hybrid drawings need no specialized numbering system. (This includes multiple artworks for one substrate.)

Every drawing should be subject to a standardized system of controlling and recording any changes to the configuration. Engineering orders, drawing revision notices and any of the usual control documents should be applied to hybrid documentation. As a matter of fact even more scrupulous attention should be paid to configuration and process control because hybrid technology, being relatively new, is evolving more rapidly than more established technologies.

9.1 ASSEMBLY DRAWINGS

The hybrid assembly drawing is usually (but not always) the top assembly drawing in the hierarchy of engineering documents. Sometimes a specification control document is created to define only the size, the electrical parameters and the part number of the finished part. Such a document is usually created when the parts will be manufactured by a vendor outside of the user's organization. However such a specification could be the top drawing of a hierarchy of drawings, in which case the assembly drawing would "sub" into it.

A hybrid assembly drawing (like any assembly drawing) should depict the completed part, specify the processes to be used, and should reference all the other documents next to it in the hierarchy of drawings. However some aspects of a hybrid assembly drawing should be pointed out.

The orientation of each semiconductor should be clearly defined. The most complete definition would be to depict the entire metalization pattern of the chip. This can be done by acquiring from the manufacturer an image of the pattern, suitable for photographing, then photographically creating the appropriate size of the image and stripping it into the place on the drawing. The entire drawing should then be reproduced into one image in order to eliminate the stripped-in pieces. Such a series of efforts is too expensive, and time consuming. It further dictates that the assembly drawing cannot be completed until the manufacturer sends the image. In most cases this is intolerable.

9.1 (Cont.) ASSEMBLY DRAWINGS

Depicting the orientation with pencil line drafting is much more desirable, but care must be taken to be sure the unavoidably abbreviated pencil drawing is truly definitive. The chips are often symmetrically shaped, and their metallization patterns are too complex to draw within the small size; even if more space were available, drawing the metallization is much too tedious.

As a minimum, all terminal pads should be shown, even if some are not wired. If the terminals are arranged in an obviously nonsymmetrical pattern, then showing this nonsymmetrical arrangement can suffice to clarify the orientation. When the terminal arrangement is not sufficient, then one noticeable feature in the metallization pattern should be depicted.

The number of one or more terminal pads should be shown in order to relate the assembly directly to the schematic. This numbering alone has sometimes been used as the only orientation for the chip. It does in fact indicate where each terminal should be, but what it does not do is tell the operator how to identify each terminal.

An additional consideration is that sometimes alternative chips may be acceptable as substitutes for the preferred ones. In such a case the orientation of the substitute chip should be made clear. This can be done by drawing a separate detail that shows the alternative chip substituted for the preferred one.

It is definitely preferred that the patterns on the substrate be depicted so that there is an obvious distinction between conductor tracks and the spaces between. This is particularly important for clarifying the wire bonding points on the substrate.

9.1 (Cont.) ASSEMBLY DRAWINGS

Pencil line drawing is usually not well suited to fulfill this criterion. A half-tone image (created from the original artwork) is far more distinguishable. As an example of the difference, in clarity between a line drawing and a half-tone image, compare Figure 9.1-1 to the image of circuit No. 2 in Section 1.8 (P. 1-43). Figure 9.1-1 is a line drawing tracing of the lower right corner of circuit No. 2.

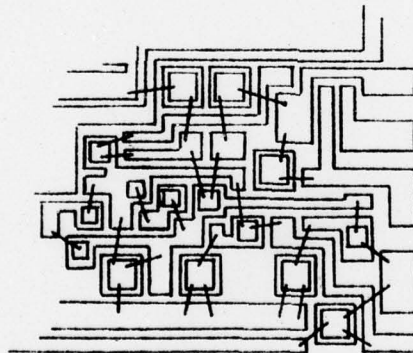


Figure 9.1-1 EXAMPLE OF A LINE DRAWING FOR A HYBRID ASSEMBLY

9.2 PARTS LISTS

Hybrid parts lists are very similar to parts lists used for other electronic parts and assemblies with only a few unique requirements. Many different manufacturers make semiconductor devices that conform to the electrical and physical parameters of military and industrial specifications but each manufacturer's chip (inside the package) may have a different configuration.

The callout of a semiconductor device should make it clear that only the chip is required; not a completely packaged transistor, diode, or integrated circuit. Using only the common "2N" or "1N" numbers for transistor and diode chips has been done in the past with resultant confusion. These numbers, used without modifying explanations, designate the complete assembly of chip and package. It should also be made clear whether or not the chip must have gold on the back side.

Because semiconductor manufacturers have been known to change the locations of terminals on an IC chip without changing the chip's part number, it is a good idea to verify the terminal positions of any IC chip before releasing the parts list for purchasing. If the chip metallization can be specified, this information should be included.

In specifying the material for substrates it is important to indicate the degree of purity required and the amount of camber acceptable.

Thin film resistor and conductor materials are typically not called out on the parts list. These materials are usually not purchased for a unique substrate but rather are purchased as bulk material. It is the process control specification that defines

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9.2 (Cont.) PARTS LISTS

the requirements for the material being used. (The same way that material would be specified for use in a plating tank.) The substrate drawing typically specifies the basic type of material and also references the process control specification.

Thick film materials should be specified on the substrate parts list. The specific vendor part numbers should be shown. The various materials specified are known to be compatible with each other and arbitrary substitutions are not allowed. When specific substitutes are acceptable they should be included. (This applies to any part on the list.)

When solder is specified on a parts list the composition and form should be made clear. When preforms are intended these typically have specific part numbers so there is usually no problem. Confusion has arisen when numbers such as "SN63" are specified. The number "SN63" is only part of a larger number defined in the military specification QQ-S-571. The complete part number indicates not only the solder composition but also includes the form of the solder and the requirements for flux.

9.3 SUBSTRATE DRAWINGS

The drawing of a substrate should define, as a minimum, the raw material and the size of the substrate, the relationship of the artwork patterns to each other and to the substrate, the materials used for each film pattern, the processes to be used in fabrication.

Many document control systems, especially computerized data control systems, create a separate parts list for the substrate detail. Whether on a separate parts list or integral with the substrate drawing, the material and size should be specified with tolerances. The percentage of purity of the ceramic should be indicated. If the substrate is to be purchased as a vendor part, the vendor's part number should be indicated along with the dimensions. (Alternate vendors and their parts numbers should be included.) The allowable amount of camber should be specified.

One area of drafting conventions has caused some confusion in the past. Confusion comes about because the usual sequences of assembly buildup is reversed for scribe-and-break substrates. The usual assembly buildup is that smaller parts are combined with other parts to make up a larger assembly. The usual drafting practices are suited to this sequence. The usual convention indicates by a matrix of rows and columns, the quantities of smaller parts required to create larger assemblies. (i.e., The system can only indicate several parts being combined into one larger part; it cannot show one part being made into several smaller ones.) When a substrate is made as one large piece then broken into several smaller ones, this reverses the usual sequence and the standard drafting conventions are not adequate for indicating this reversed sequence.

9.3 (Cont.) SUBSTRATE DRAWINGS

One way to avoid confusion is to create two drawings, one showing the fabrication of the larger multiple-image substrate, and the other showing the finished smaller substrate but indicating that it is to be made from the other part. This method has the disadvantage of requiring an additional drawing.

Sometimes the question has been resolved by following the philosophy that the drawings need only define the finished product and that the manufacturing group has the option of choosing the fabrication methods. In this method the substrate drawing ignores the fact that the substrate is fabricated through an interim configuration. This interim stage is not defined and no identification number is assigned to it. This philosophy, while fulfilling the primary goal of engineering documentation, goes against the grain when engineering control of the processes is intended. A further disadvantage could result if the substrate drawing depicts a single substrate but multiple images appear in the 1x scale master pattern. The difference might cause confusion.

Another way to resolve the questions is to show only the finished part on the substrate drawing, and to follow the usual method of assigning, on the parts list, a dash number to each fabricated part.

The parts list would then show an assembly buildup of the larger part being "subbed" into the finished part. However, no indication is given of the quantity of larger parts required for the smaller part; a symbol is used instead. This symbol is a cross reference to a note that explains in clear language that a certain quantity of the finished parts is to be made from the larger part. (Of course, each part would be referred to by the appropriate dash number or item number.)

9.3 (Cont.) SUBSTRATE DRAWINGS

A delicate subject often arises when complete documentation is intended: the question of the proprietary nature of many company-developed processes. Many more of these proprietary processes are involved in the substrate fabrication than in the subsequent assembly processes. The substrate drawing need not specifically define each process. (This would be a gross inefficiency if repeated on each substrate drawing.) The substrate drawing can reference the separate controlling document for each process or it can reference only the manufacturing operations traveler, which will in turn reference each process control document and the sequence in which they are to be applied. The process control documents can be classified as company proprietary. This proprietary status is respected by military procurement agencies, if the appropriate indication of this status is shown as defined in MIL-STD-100. (MIL-STD-100 dictates that whenever a proprietary document is referenced on another document, that status must be so indicated. One note is sufficient to indicate this status for many such documents referenced on one drawing.)

The substrate drawing must make clear the proper orientation of the film patterns to each other and to the substrate. In most cases this can be satisfactorily accomplished by depicting the conductor and resistor patterns shaded in various ways, with the bare ceramic and the dielectric shown as clear areas outlined by pencil lines.

The patterns can be photographically reproduced in half- or full-tones from the original artwork. Half-tone for conductors and full-tone for resistors is most common. If more than one resistor paste is used for a thick film substrate, it is convenient but not necessary to have each paste distinguishable from the others.

9.3 (Cont.) SUBSTRATE DRAWINGS

The resistor design data information (which should be included or referenced on the drawing) will clarify which paste is required for each resistor. However, the drawing must make clear the appropriate artwork to be used for each type of paste.

In the case of multilayer substrates, again it is convenient but usually unnecessary to depict each separate layer. If alignment targets are included in each layer, the relationship of the patterns will be obvious, and only the top layer need be shown for proper orientation to the ceramic. Where alignment targets cannot be used, vias, via-fill metallization patterns, and corresponding pads can usually provide sufficient guides for alignment. A good reason not to show each layer is that if subsequent changes are made to the artworks, the need to change the substrate drawing is minimized.

A cross-section view of a portion of the substrate should be included to show the sequence of layers. This view should indicate which artwork is used for each layer. The section view need not be dimensionally precise; it can be noted that the view is intended to show sequence only and that no scale is intended. The note should also explain that vias and conductors shown in the section view do not represent the exact locations on the actual part. This section view can be almost universal for all multilayer substrates. It can be traced onto each new drawing, and the top layers added or deleted as required.

The distance from the edge of the substrate to the pattern should be dimensioned if no alignment targets are available and some of the layers occupy only a portion of the substrate. Such cases are an exception to the general statement that individual layers usually need not be shown.

9.4 LAYOUTS

Because the layout is not part of the set of engineering documents released for manufacturing, there are a variety of attitudes about how much control should be maintained on the layout. These attitudes range from treating it as only a sketch and imposing no controls to placing all the controls usually placed on manufacturing drawings. A compromise between these two extremes has proven to be useful.

For a single layer design, after the assembly drawing has been created, that assembly drawing depicts everything that the layout does, therefore preservation and control of the layout is often not emphasized. For a multilayer design, the assembly drawing typically shows only the top layer; the layout is the only document that shows the interrelation of all the layers and the components. If, after the original design has been completed, subsequent changes are required to a multilayer substrate, the original design layout is very useful.

Layouts can be placed under an abbreviated document-control plan that provides safekeeping and configuration control while eliminating the usual engineering orders and other similar paperwork.

The original layout should have a document number that relates to the assembly drawing, using the assembly drawing number with a prefix added, has been effective. It should have provisions for approval signatures and should have the usual revision block in the upper right-hand corner. After the official set of engineering drawings has been completed, the layout can be placed in storage and filed numerically.

9.4 (Cont.) LAYOUTS

Whenever needed, it can be checked out from storage. The changes can be made and a revision letter and date entered in the revision block. At least one approval signature should be required for a change, and that signature could be entered in the revision block. No E.O's or similar forms need be written to authorize changes to the layout. These authorizing forms are required for the officially released documents. Since the layout is not used for manufacturing, there is seldom any need to make prints of it. All layouts (but especially those being stored for future use) should be created on stable material to insure accuracy.

9.5 ARTWORK (AS CONTROLLED DOCUMENTS)

It is often the case that a glass or film "master pattern" is created at 1x scale. It is from this master that the working thin film masks are made or from which the thick film screens are made. When such a 1x master is created, the question may arise about the status of the enlarged (usually 20x scale) artwork. The question centers around which one is the true master.

Aside from the semantics of the word "master", there need not be a problem. To make a distinction between the two, the number of each one can have a different prefix. Each is useful and should be stored for safekeeping. Either can be treated as the official document. Change authorizations (E.O.'s or change notices) should be directed to the one selected as official, thereby making all the paperwork consistent. The other can be treated as a tool.

9.6 MARKING DRAWINGS

One common method of marking a hybrid is to screen print the universal portion of the marking and to rubber stamp the variable portion (i.e., serial number, lot number, manufactured date). When printing or any other method is used and that method requires an artwork, the artwork can be part of the set of official documents.

The marking artwork can have a document number and can be controlled the same as other documents in the set. The marking material (ink, paint or other) can be specified on the assembly drawing or in a process control document.

9.6 (Cont.) MARKING DRAWINGS

An alternative is to verbally specify, on the assembly drawing or on a separate document, the size and type of characters, as well as the material to be used for marking.

9.7 PROCUREMENT CONTROL DOCUMENTS

The purpose of any procurement control document is to specify the parameters of a purchased item, and/or the acceptable sources of that item.

Of the components commonly used in hybrids, the one most likely to be a candidate for a specification control drawing or a source control drawing is the naked I.C. chip. There have been instances in which semiconductor manufacturers have changed the locations of the terminal pads on a chip, without changing the part number. Purchasing such a part by specifying only the vendor part number could result in the parts being unusable in the hybrid. If there is any question about the specific physical or electrical parameters of a component, then a specification control drawing can be created which should delineate each requirement.

Transistor and diode chips rarely have a problem with terminal locations because the diode has only one terminal and the transistor only two. The transistor chip can typically be rotated to accommodate any wire-bonding arrangement. The diode requires no particular orientation.

9.8 ON-LINE ASSEMBLY-AID DRAWINGS

The official assembly drawing shows the requirements for the finished part, but typically does not contain sufficient

9.8 (Cont.) ON-LINE ASSEMBLY-AID DRAWINGS

instructions for the on-line operators. For this reason, an assembly-aid drawing is often created by the manufacturing group.

The assembly-aid should include all instructions required by the operators, along with a picture of the components and wires. The picture is sometimes a photograph of the first unit built. This method, however, means that the on-line drawing cannot be created until after the first unit is built. If the picture on the assembly drawing has sufficient clarity, this picture can be used instead of a photograph.

Whichever picture is used should be at a scale close to the magnification seen by the operator when looking through the microscope. If the microscope view and the assembly-aid picture are equivalent sizes, this minimizes the need for the operator to make visual adjustments when looking from one to the other. Such minimal adjustment reduces errors and also reduces the strain on the eyes of the operator.

If possible, the on-line drawing should show the actual metallization on each semiconductor chip. Since no paperwork is required to change this drawing, the semiconductor metallization images can be pasted in the border area of the drawing. One image of each type of chip is usually sufficient.

9.9 MULTILAYER SUBSTRATE CHECK-OUT LIST

Each multilayer substrate needs to be tested to determine that there are no electrical shorts or open circuits below the dielectric material or within the vias. The method of testing is to apply probes to various points on the conductor tracks and then check the connection or lack of connection between the probe points. The list of such points along with their required interconnections is called a "substrate check-out list" in this text.

It is not sufficient for the list to show only the points that require interconnection. Many points need proof of no-connections, such as the points where two conductor tracks that cross are separated by only one layer of dielectric material. (Double printing and firing of the dielectric is not a guarantee against shorts between conductor layers.)

Before the list can be made, each probe point must be assigned a designation in order that it can be specified on the list. One commonly used way of making the assignment is to take the designations directly from the schematic. Each component on the schematic already has a designation and most have distinguishable terminals. Using this method, the substrate bonding pad for the fifth terminal of the second I.C. chip would be called U2-5; the emitter bonding pad for the first transistor would be called Q1-E; the substrate exit pad that is to be wired to package pin number 27 would be called Pin 27. For components having undistinguishable terminals (such as resistors), the terminals would be assigned arbitrary numbers.

A drawing is then needed to show where these designated points are located on the substrate. The assembly drawing of the hybrid can serve this purpose if all the component terminal numbers are shown.

9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST

However, while using the schematic designations and the assembly drawing makes it easy to generate the check-out list, this method of assignment is not the best suited to manually performing the check-out tests. Since the orientation and location of the components on the substrate is rarely consistent or sequential, the operator must randomly search the assembly drawing to find the probe points. A sequential arrangement on the substrate would make this search much easier.

One method of assignment that has been used is not time consuming while creating the list, yet does aid the check-out operator. This method is to assign all component designations in a sequence according to the location on the substrate; and then to repeat that assignment on the schematic. This method, while improving the check-out process, delays completion of the schematic, and could delay completion of the parts list. Secondly, this still would not provide consistent orientation of each component.

Another method, better suited to manual check-out, is to arbitrarily assign a designation to each probe point with no regard for components. Such an arbitrary assignment if made in a logical sequence is much easier for the operator to follow. The drawing used to define these points could be the detail drawing of the substrate if the point designations are drawn on the conductor pattern of the top layer.

Whichever drawing is used to define the probe points, that drawing should be a half-tone image of the conductor track artwork. It should not be a line-drawing of the artwork because on such a line-drawing it is very difficult to distinguish the conductor

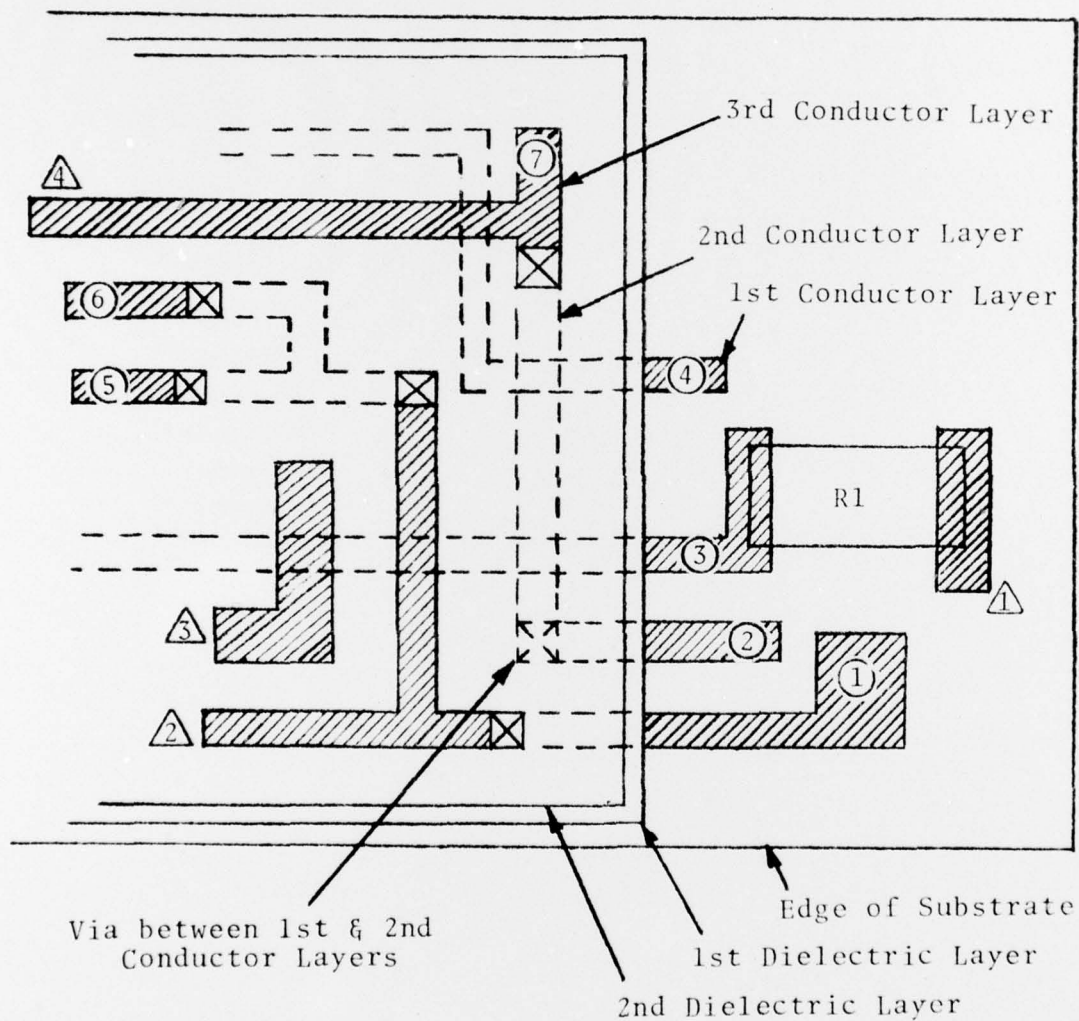
9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST

tracks from the spaces between them. (An exception to this rule would be such a pattern as shown in Figure 7.7-4 in which only wire bonding and exit pads appear on the top layer.)

Not every component terminal point needs to be probed. If a conductor track does not cross another conductor with only one dielectric layer between, and also does not need a via to connect it to another layer, it does not need to be probed. Such a track could be on the top layer only or in an area devoid of multilayers. For automatic check-out, such distinctions are usually not significant; but for manual testing the check-out list should be as short as possible. Figure 9.9-1 shows some examples of probe point selections.

While it is true that assigning sequential designations and eliminating unnecessary probe points is more time-consuming while creating the list, this extra time should be compared to the fact that the check-out list is only created one time, but that the check-out process will be performed many times.

9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST



Note: Only circles are probe points; triangles are for reference in the text.

Figure 9.9-1 EXAMPLES OF PROBE-POINT SELECTIONS

9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST

No probes are required at points $\triangle 1$, $\triangle 2$, $\triangle 3$ and $\triangle 4$. The point labeled $\triangle 1$ is on a track that is entirely unassociated with the multilayer area of the substrate. Point $\triangle 2$ is not necessary because checking the connection between $\textcircled{1}$ and $\textcircled{5}$ tests all the vias in between the two. Point $\triangle 2$ would only repeat the test of one of these vias. If no connection exists between $\textcircled{1}$ and $\textcircled{5}$, the part is rejected so it does not matter which via or track is at fault. Point $\triangle 3$ is separated from $\textcircled{3}$ by two layers of dielectric so no proof of isolation is required. Two layers of dielectric means four separate print-and-fire cycles of dielectric material between $\triangle 3$ and $\textcircled{3}$. This is considered sufficient without proof. $\triangle 4$ is electrically the same point as $\textcircled{7}$ so no probe is required. If a break exists in the track between $\triangle 4$ and $\textcircled{7}$ it can be seen during visual inspection.

The required tests are between $\textcircled{1}$ and $\textcircled{5}$, $\textcircled{1}$ and $\textcircled{6}$, $\textcircled{2}$ and $\textcircled{7}$. The required proof of isolation is between $\textcircled{2}$ and $\textcircled{3}$, $\textcircled{2}$ and $\textcircled{4}$. No proof of isolation is required between $\textcircled{1}$ and $\textcircled{2}$ because they do not cross each other. No proof is required between $\textcircled{1}$ and $\textcircled{3}$ because they are separated by two layers of dielectric, where they cross.

Figure 9.9-2 shows examples of two types of check-out list entries. The list should be part of a multiple-page document that begins with a cover page containing the title block, revision block, and approval signatures; and continuation pages that show the document number, cross references to any additional applicable drawings, and explanations of the purpose and procedure for performing the tests.

9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST

FROM	TO									
The following points on the substrate (located per drawing) require interconnection between each point shown in the "FROM" column and each of the points shown in the corresponding "TO" columns.										
1	5	6								
2	7									
Proof is required that no connection exists between the following points shown in the "FROM" column and each of the points shown in the corresponding "TO" columns.										
2	3	4								

Figure 9.9-2 EXAMPLES OF CHECK-OUT LIST ENTRIES.

When substrates are tested using automatic check-out equipment, contact is made to all the probe points simultaneously using a multiple probe assembly. The probes are wired through a harness to a connector that plugs into the check-out equipment. The equipment compares one point to every other point.

When automatic check-out is to be used, another consideration needs to be made. The machine only "recognizes" the pin numbers of the connector that plugs into the machine. The machine indicates errors using its own pin numbers as designations. It does

9.9 (Cont.) MULTILAYER SUBSTRATE CHECK-OUT LIST

not print-out the designations assigned to the probe points on the substrate. Either a cross-reference list is needed to relate the connector pin numbers, to the substrate points or the connector pin numbers should be used as the designations for the corresponding probe points. Without some form of cross reference the machine "language" cannot be related to positions on the substrate.

When automatic equipment is used, only the required connections need appear on the list. The list need not indicate tests for proof of isolation because the machine compares each point to every other point. However, this does not eliminate the need for a probe to be placed on each of the "possible-problem-tracks."

9.10 PROCESS CONTROL SPECIFICATIONS

Two types of documents typically dictate the processes to be used in manufacturing. One type is the operations traveler and the other is the process specification.

The operations traveler is usually generated by the manufacturing group, but sometimes the engineering group creates this document and releases it as one of the set of engineering documents. The traveler establishes the sequence in which the operations are to be performed and references the appropriate process specification for each operation. It has provisions for each operator or inspector to sign after completing the indicated operation. It also provides space for failures, rejects, and rework to be indicated.

9.10 (Cont.) PROCESS CONTROL SPECIFICATIONS

An operations traveler accompanies each serial-numbered part through all the assembly and testing processes, and when the part is completed and accepted, the traveler contains a history of all the activities associated with that particular part. After the part is shipped, the traveler should be filed for safekeeping.

The process specification documents define the equipment, materials, and techniques to be used in each manufacturing process. These documents are the most important ones created by a hybrid manufacturer. Because they describe the details of each manufacturing process, they are typically regarded as proprietary documents.

SECTION 10 DEFINITION OF TERMS

The following are definitions of terms commonly used in micro-electronic technology.

<u>TERM</u>	<u>DEFINITION</u>
Angstrom - Symbol (\AA)	A unit of linear measure. $10,000 \text{\AA} = 1$ micrometer.
Ball Bond	A thermocompression bond of a gold wire with a ball of gold on the end of the wire.
Bonding Pad	In a metallized pattern, a bonding pad is the area designated for bonding wire.
Camber	The amount of warpage in a substrate. Typically specified in units of "mils per inch." (Mils of curvature per inch of length.)
Die	A semiconductor chip. Plural is dice.
Die Attach	The attachment of a semiconductor die.
Eutectic	An alloy is eutectic if its component materials are in the proportion that produces the lowest melting point. (80% gold, 20% tin is the proportion that has the lowest melting point for an alloy of these two materials.) The melting temperature is also referred to as the eutectic point.

SECTION 10 (Cont.) DEFINITION OF TERMS

<u>TERM</u>	<u>DEFINITION</u>
Eutectic Attach	A method of attaching a semiconductor chip by applying heat while scrubbing the chip onto the gold mounting pad. The silicon and gold form a eutectic at the interface.
Firing	The process of heating thick film materials to cause the vehicles to evaporate and the remaining solid particles to adhere to each other and to the substrate.
Hermetic Seal	A seal that is gas tight.
Hybrid	A shortened version of the term "hybrid microcircuit." A miniaturized electronic assembly involving an insulating substrate on which are deposited conductive, resistive, and dielectric patterns and to which electronic components are usually attached.
Ink	Thick film material in liquid state. Term used synonymously with the term "paste".
Mask	The glass or film containing the 1x scale pattern which will be applied onto a substrate or wafer.

SECTION 10 (Cont.) DEFINITION OF TERMS

<u>TERM</u>	<u>DEFINITION</u>
Microinch - Symbol (μ in.)	A millionth part of an inch.
Micrometer - Symbol (μ m)	One millionth part of a meter. Equal to .0000394 inches.
Mil	One thousandth of an inch. Equal to 0.0254 mm.
Moly-Tab	A gold-plated molybdenum tab on which a semiconductor chip is some- times mounted. Used to provide heat sinking of eutectic attach and advantage of solder attach to substrate.
Paste	Synonymous with the term "ink" when referring to thick film materials which are screened on substrates. Thick film pastes usually consist of metals, metal oxides, solvents, binders and crystalizable glass frit.
Photoresist	The light-sensitive coating material in which a pattern is created in order to protect portions of a surface from etching or plating.

SECTION 10 (Cont.) DEFINITION OF TERMS

<u>TERM</u>	<u>DEFINITION</u>
Screen Printing	The process of applying thick film paste through a screen onto a substrate.
Screening	Same as screen printing.
Sputtering	A deposition process (conducted within a vacuum chamber) in which the material to be deposited is bombarded with ions thereby knocking off molecules which deposit themselves onto other surfaces.
Stitch Bond	A series of point-to-point bonds made with a continuous wire.
Substrate	The base material (usually flat) onto which an electric circuit pattern is created. In hybrids it is the ceramic base. The expression "metallized substrate" is often used to distinguish the substrate with the pattern applied from the bare ceramic substrate.

SECTION 10 (Cont.) DEFINITION OF TERMS

<u>TERM</u>	<u>DEFINITION</u>
T.C. Bond	Thermo-compression bond. A method of attaching a wire by applying heat and pressure.
T.C.R.	Temperature Coefficient of Resistance. The change in resistance per degree of temperature change. Expressed as parts-per-million per degree centigrade (ppm/°C).
Thermal Evaporation	A deposition process (conducted within a vacuum chamber) whereby the material to be deposited is heated to cause the material to vaporize and deposit itself onto other surfaces.
Thick Film	The film of conductive, resistive, or dielectric material deposited onto a substrate by a screening method.
Thin Film	The film of conductive, resistive, or dielectric material deposited onto a substrate by a vacuum deposition method.
Trimming	The process of modifying the geometry of a resistor or capacitor in order to adjust the component's value.
Ultrasonic Bond	The attachment of a wire by applying pressure and ultrasonic energy.

SECTION 10 (Cont.) DEFINITION OF TERMS

<u>TERM</u>	<u>DEFINITION</u>
Via	The opening in an insulating layer, through which electrical contact is made to the conductive patterns above and below the insulating layer.
Wafer	The thin slice of silicon or other base material on which multiple semiconductor devices are fabricated simultaneously.
Wire Bond	The bonded (deformed) portion of an attached wire. Often used as a verb (i.e., to wire bond).
Yield	The percentage of acceptable final products compared to the amount starting into the manufacturing cycle. (If out of 50 parts starting into the manufacturing cycle, 40 pass final acceptance, then the yield is 80%.)